IBM Customer Engineering

Instruction-Reference

Preliminary Edition

1410 Core Storage

R23-2555

PREFACE

This manual contains the instruction material for the various models and capacities of core storage used with the 1410 Data Processing System. Reference information and servicing procedures are included. This manual obsoletes the core storage sections of the Customer Engineer Manual of Instruction for 1410 Data Processing System - Form 225-6549-1.

SAFETY

Although the highest DC voltage present in the core storage modules is +60 volts, power supply AC voltages are present in the expanded memory models and at the bottom of the modules for the blowers. When it is necessary to work on the power supplies or blowers, remove all power from the system. If servicing the power supplies with power on is impossible to avoid, BE EXTREMELY CAREFUL because the input voltages to the power supplies are potentially dangerous.

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TABLE OF CONTENTS

1410 CORE STORAGE

The core storage section of the IBM 1411 Central Processing Unit provides immediate, random access to data and instructions necessary for the operation of the 1410 Data Processing System. The 1411 is available in five models of different memory capacities. The model 1 has 10,000 positions of storage. The models 2 through 5 have 20,000 , 40,000 , 60,000 , and 80,000 positions respectively. Also a 100,000 position capacity is available by installing the 7251 Model 1 Additional 60K Memory.

Each position of core storage has a five-digit decimal address that defines one of the 100,000 possible locations. The models of 1411 and their associated addresses are:

Model 1	00,000 - 09,999
Model 2	00,000 - 19,999
Model 3	00,000 - 39,999
Model 4	00,000 - 59,999
Model 5	00,000 - 79,999
7251 Model 1	00,000 - 99,999

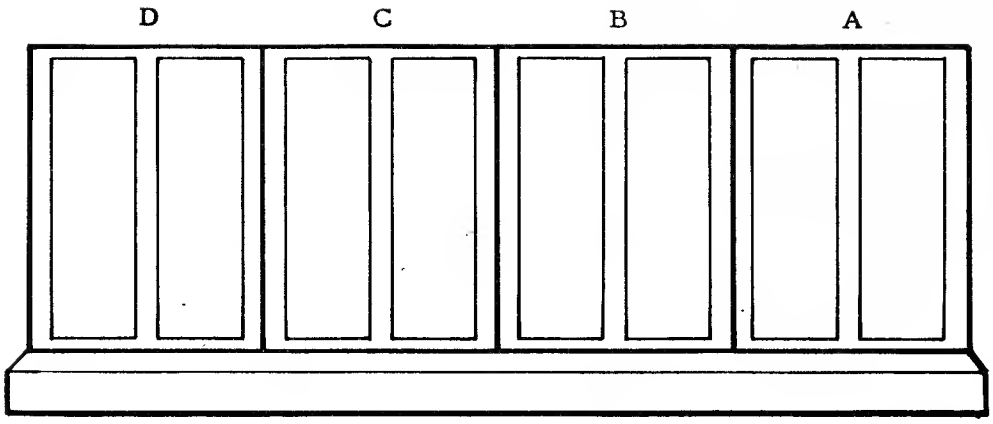
Each of the possible addresses locates one binary coded decimal (BCD) character. . A BCD character requires six data bits plus a seventh check bit. Each location also has an eighth bit called the word mark bit. Therefore, each address locates one eight-bit character.

PHYSICAL LAYOUT

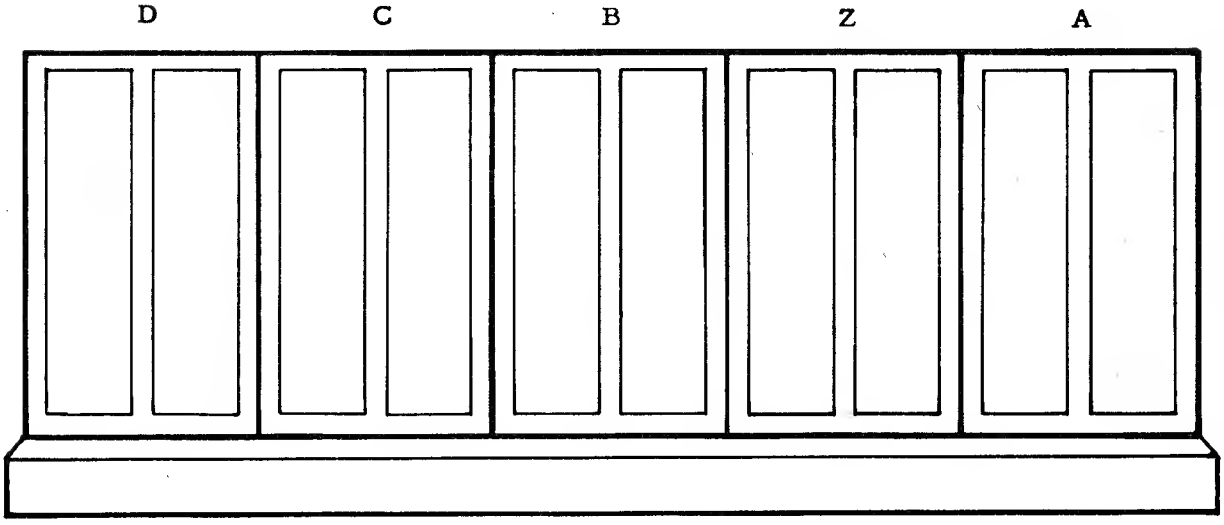
In the 1411 Models 1, 2, and 3, the core array and its associated circuits are located in Module B. A Model 4, 5, or the 7251 Model 1 uses two Modules: a B Module similar to the model 3, plus a Z Module that is added

between the A and B Modules (Figure 1). The Z module is necessary for storage capacities above 40,000 positions.

The cores are wound on planes of 100 X 100 cores for a total of 10,000 per plane. The core array for the smallest of the available models, model 1, has eight of these planes or a total of 80,000 cores. The larger capacities are built by adding multiples of eight planes for each group of 10,000 positions needed.



Model 1, 2, or 3



Model 4, 5, or 7251 Model 1

Figure 1 1411 Module Layout

Core Storage Fundamentals

Ferrite Cores As Storage Devices

Magnetic core storage uses as a storage medium a very small doughnut-like ring composed mostly of iron. Ferrite cores store bits of information, either data or instructions, in the form of magnetic flux. Each core has four wires passing through it (X, Y, inhibit, and sense wires) which control the complete operation of the core. See Figure 2.

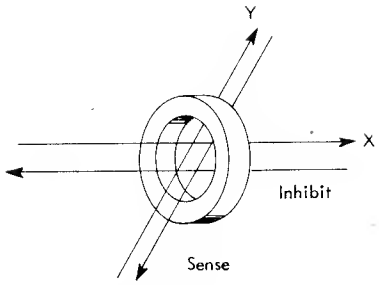


Figure 2. Ferrite Core with Windings

The ferrite cores are wound in frames called core planes. Core planes are stacked to form a core array.

The considerations in core storage are selection, reading, and writing. A network of X and Y switching circuits satisfies all three considerations. The desired character address is held in a register composed of triggers. The switching circuits use the register outputs to select the position in storage and perform reading and writing. Diode decoders, switch cores, and coincident currents are employed in the switching circuits. Through the switching device any character position in core storage can be selected for reading and writing.

The Ferrite Core

Physical Properties

Ferrite core manufacture is carefully controlled so that cores will have correct and uniform characteristics. The raw materials used are oxides of iron and magnesium, along with manganese carbonate. This mixture is pulverized and heat treated, a binder is added, and the mixture is stamped into ring-shaped cores. Additional heat-treating steps are required to complete the manufacturing process.

Since the physical size and manufacturing processes affect the magnetic behavior of the cores, the magnetic properties of the cores are carefully checked before they are used in the machine.

Magnetic Properties

The ferrite core is a bi-stable storage device. It has the ability to store a bit of information in the form of magnetic flux. The ferro-magnetic properties of the core permit it to be magnetized by applying an external magnetizing action or magnetomotive force (MMF). Wires that carry direct electric current are inserted through the core to generate the MMF. Once the core is magnetized, it retains the magnetic flux even though the MMF is removed. The core remains magnetized until again operated on by an external force. The ability of the core to retain magnetic flux is the property that makes it useful as a storage device.

Under static conditions the ferrite core is magnetized in one of two possible stable states (hence the term bi-stable). In one state the magnetic flux lines are clockwise inside the core. In the other, the magnetic flux lines are counterclockwise inside the core. The state of the core at any instant depends on the last previous action caused by the external MMF. Under static conditions ferrite cores are never magnetically neutral.

The two states of the cores are used to represent binary bit information. With the magnetic flux inside the core in one direction, it is set and contains a 1. With the magnetic flux inside the core in the reverse direction, it is reset and holds a 0. Notice that each core has two flux states. The actual polarity of the magnetic flux inside the core is of no consequence. The core storage units utilize only flux reversals. The logic

applied to core storage is this: If reading from a core reversed its flux state, it contained a 1; if reading from a core did not reverse its flux state, it contained a 0. The polarities are fixed relative to each core by the driving circuits feeding the cores. The exact polarity of the core at any time need not be determined.

Reversing the flux state of the ferrite core is called "flipping" the core. This term applies to both cases (0 to 1 and 1 to 0).

The external MMF for driving the ferrite cores is generated by wires carrying direct electric currents. In a wire with a direct electric current flow, a field of magnetic flux is generated, encircling the wire. The polarity of the flux lines can be determined by applying the left-hand thumb rule for current flow. The magnetic flux density is directly proportional to the amount of current flowing. Reversing the current flow in the wire reverses the flux line direction, but the magnetic flux density is again directly proportional to the amount of current flowing. The polarity and density of the magnetic flux generated around a conductor are therefore dependent on the direction and amount of current flow.

The magnetism produced as a magnetomotive force applied to a core can be expressed graphically. The graph of flux density (B) versus magnetizing force (H) is called a B-H curve or hysteresis loop (Figure 3). For an electrical coil H = NI where N is the number of turns in the coil and I is the current. In ferrite core storage the wires pass through the core only once; therefore, N = 1. With single turn windings, the magnetomotive force is numerically equal to the current; it is simpler, therefore, to express H in terms of I.

An ideal ferrite core would have a rectangular B-H curve; this condition does not exist, however. A typical B-H curve is shown in Figure 3.

The ferrite core operates along the path of the B-H curve. Consider a core initially with no magnetic flux (B = 0). String the core on a conductor. Passing current through the conductor generates a magnetomotive force, magnetizing the core. The path followed is from A to J as shown by the dotted line in Figure 3. After reaching point J the ferrite core becomes saturated with magnetic flux. Any increase in I (current) beyond point J causes little increase in the flux inside the core. The value of current necessary to just saturate the core is referred to as full current (I). When I is reduced to zero, the flux state of the core resides at point L. Application of −I (reversing current in the conductor) flips the core along the path L to N. (Notice that ½I is not sufficient to flip the core.) Removal of the −I lets the core reside in the flux state represented by point Q. Application of +I flips the core along the path from Q to J. Removing the +I lets

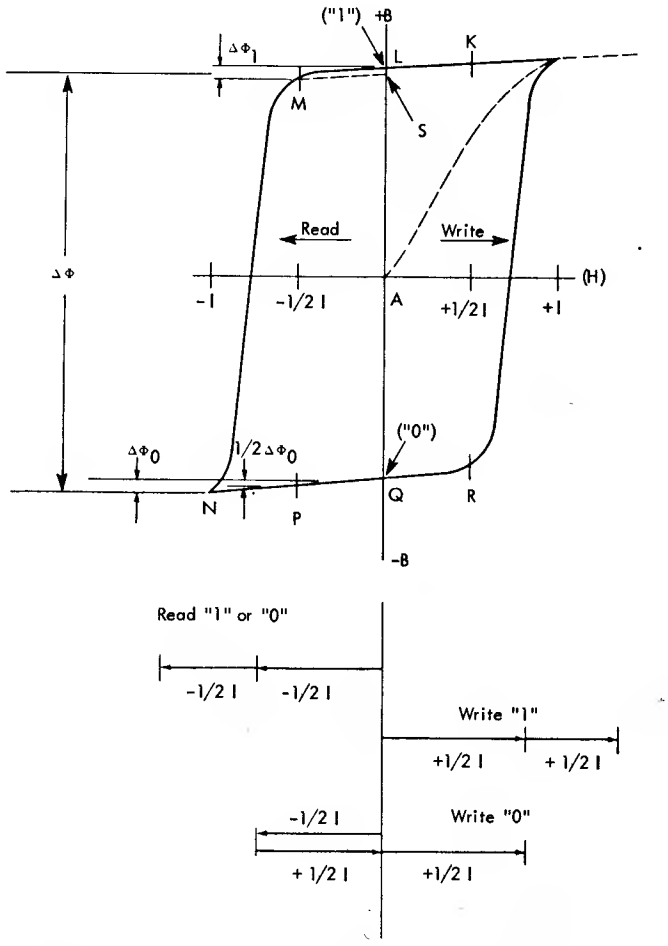


Figure 3. Core Outputs and Core Currents

the core again reside at point L. When the core is in the flux state as represented by point L, it is arbitrarily said to be in the 1 flux state. Point Q represents the 0 flux state.

It is essential that the core be sensitive to application of +I and −I but insensitive to applications of +½I, and −½I. The following table shows the paths followed for the application and removal of the four currents (Figure 3).

Current Pulse Applied	*Resulting Path (Core Holding 0)*	*Resulting Path (Core Holding 1)*
−I	Q to N, back to Q	L to N, N to Q (flips)
−½I	Q to P, back to Q	L to M, back to L (app)
+½I	Q to R, back to Q (app)	L to K, back to L
+I	Q to J, J to L (flips)	L to J, back to L

The following conclusions can be drawn:

1. +I is required to flip the core from the 0 to 1 flux state.

2. −I is required to flip the core from the 1 to 0 state.

3. Application of +½I and −½I cannot flip the core, regardless of its flux state.

The core never comes to rest in a neutral flux state (B = 0).

To take information from a core, the core is read. Any core selected for reading has a full −I applied to it. Current in the minus direction is, therefore, called read current (Figure 3). Putting information into a core is called writing into it. The selected core has a full +I applied. Current in a plus direction is, therefore, called write current.

The directions chosen for read and write currents are arbitrary. The important fact to note is that the read current and the write current magnetomotive forces have opposite polarities as felt by the core.

Writing a 1 into a core stores flux with 1 polarity. Reading from the core reverses the flux and resets the core to 0. A change of flux state during reading is detected by a sense winding through the core. Thus, a rapid rate of change of flux is used to interpret information stored in cores. It follows that the direction assigned to read and write currents must remain fixed with respect to each core. This is fixed by the circuits that provide read and write current to the ferrite cores.

Ferrite core flipping is a function of both time and MMF. It requires approximately 1 μs to flip a ferrite core with a full current pulse applied.

Ferrite Core Plane Windings

Four varnished wires pass through each ferrite core. The cores are supported by the wires and wound in rectangular arrays called core planes. Figure 4 shows an enlarged layout of a small core plane. The windings are:

1. One X winding for each horizontal row.
2. One Y winding for each vertical row.
3. A sense winding common to all cores in the plane.
4. An inhibit winding, parallel to the X winding common to all cores in a plane.

A ferrite core is mounted at the intersection of every X and Y winding. The four windings control the complete operation of the ferrite cores in the plane.

Only one core in a plane can be selected during any one cycle. The selected core is read from during the read portion of the cycle. The same core is written into during the write portion of the same cycle. This concept is important. The selected core in a plane is first read from and then written into during the same cycle.

A coincident current selection method is used for reading a core from a plane. Consider two parallel wires through a ferrite core (Figure 4). Let 270 milliamperes of current be flowing in the same direction

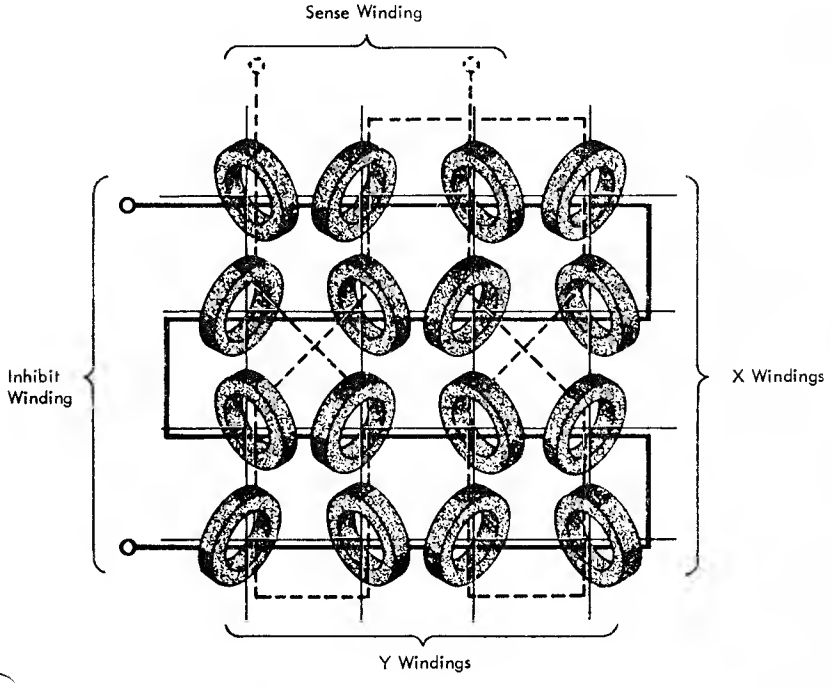


Figure 4. Core Plane Section

on each. The resulting MMF's from each wire are additive. The net effect is equivalent to one wire carrying 540 milliamperes of current. Now move one of the wires 90° with respect to the other and have the ferrite core at the intersecting point (Figure 5). With the current flowing as shown, the MMF's of the two wires are additive at the crossover point. Thus the force felt on the core is the result of 540 milliamperes of current. The MMF from full current forces the core to flip. Reversing the current in both wires sets up a MMF with opposite polarity. This force reflips the core. Coincident current is the additive effect of two currents in perpendicular wires at the intersecting point.

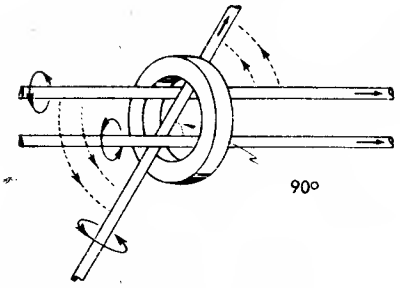


Figure 5. Coincident Current

X and Y Windings

The X and Y windings establish coincident current for selecting and reading a ferrite core from a plane. Only one X and one Y line are used during one cycle. The selected ferrite core is located at the intersection of the X and Y drive lines. Each drive line carries ½ read current at read time. (See arrows in Figure 6.) The coincident read current at the intersection of the X and Y lines applies full read current to the selected core. During write time the same X and Y lines are used. The current flow is ½ write current on each wire (opposite the arrows shown). This applies full write current to the selected core. By controlling the X and Y drive lines, any core in the plane can be selected. Using the coincident current method for selecting cores, a relatively small number of X and Y drive lines can control a large number of cores.

Only one core in a plane is fully selected for reading and writing, but other cores are half-selected. These cores feel half currents during reading and writing. All cores on the X and Y drive lines used, except the selected core, feel half current. In Figure 6, three cores on the X wire and three cores on the Y wire are half-selected. These cores are shown cross-hatched. Because ½I cannot flip a core, the half-selected cores are

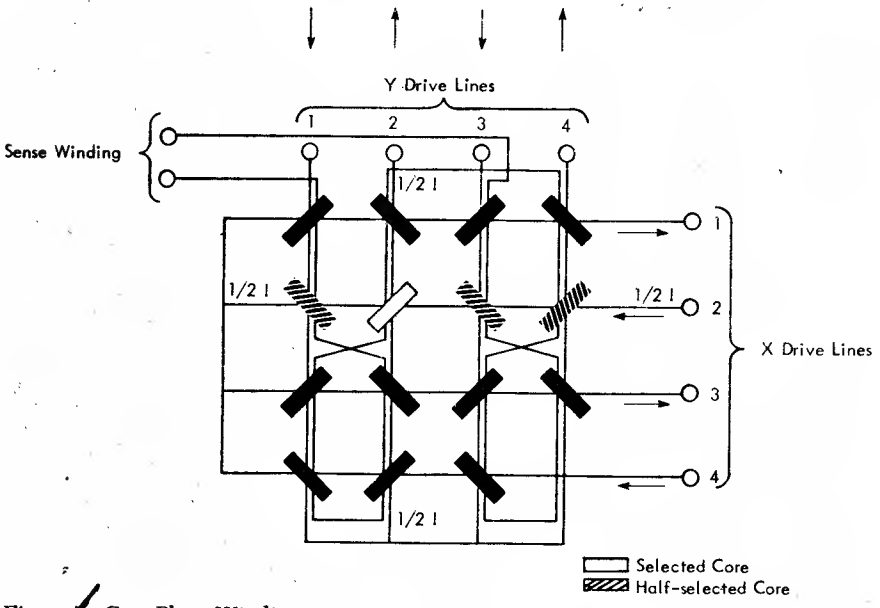


Figure 6. Core Plane Winding

ignored. Because ferrite cores are not ideal in their characteristics, half selection produces some noise output which can be bothersome on read-out.

The X and Y windings thread back and forth through the ferrite core planes from the bottom to the top of the array. The windings begin in the matrix switch core, thread through the array, and terminate in resistors.

Sense Winding

The sense winding interprets the information stored in the cores. Since information is stored in binary bit form, the problem is simply to decide whether the core holds a 1 or a 0 prior to reading.

The sense winding passes through every core in an electrical plane (Figure 7). Because only one core in a plane is interrogated during a cycle, one sense winding is adequate to interpret the information stored in all the cores in one electrical plane.

The selected core has coincident read current applied to it during read time. If the selected core holds a 1 it is flipped to 0. This causes a large flux change in the core ($\Delta\phi$ in Figure 13). The large flux change cuts the sense winding, inducing a large pulse on it. If the selected core held a 0 before the read current was applied, only a little change in flux inside the core is noted ($\Delta\phi_0$ in Figure 13). This induces only a small pulse on the sense winding. Thus, the status of the core before reading is determined.

The sense winding feeds a sense amplifier. The sense amplifier increases the amplitude of any pulses induced on the sense winding. If the core held a 1, a pulse is present at the output of the sense amplifier, and the ferrite core is flipping. Time sampling is necessary because at points in the cycle, large unwanted noise pulses are induced on the sense winding. To eliminate recognizing unwanted noise as a bit, the sense winding is sampled for a bit only at read time.

Inhibit Winding

The inhibit winding controls writing in a ferrite core plane. Current on the inhibit winding is called inhibit current. Inhibit current is effectively ½ read current. It is used during the write portion of the cycle.

A write operation is always preceded by a read operation. The read operation resets the selected core to a 0 flux state. On the following write operation, full write current is applied to the selected core by the X and Y windings. The problem is to control write current to write a 1 or a 0.

If a 1 is to be stored in the core, no problem exists; no current flows on the inhibit winding, and the full write current applied to the selected core writes a 1 into it.

Possibly the character being written has a bit structure such that a 1 is not to be written in the selected core. Then, the effect of the full write current must be blocked from writing a 1. This is done by causing inhibit current to flow on the inhibit winding. The duration of inhibit current flow overlaps write current flow. The net effect felt by the core is the result of full write current plus ½ read current. (It will be recalled that read and write currents have opposite polarity.) The selected core feels only ½ write current. As a result, the selected core remains at 0 and no cores in the plane flip.

The inhibit winding is common to all cores in the core plane; it is used, therefore, to control writing in every core in an electrical plane.

Core Array

Eight cores are needed to store one character in BCD form. Each core stands for one of the eight bits (1, 2, 4, 8, A, B, C, WM).

The core array has 8 planes corresponding to the 8 bits. Each plane has a sense winding that goes through every core on that plane (Figure 2.1-2). The number of cores on each plane determines the number of characters that can be stored.

Read

To read a character out of storage, the appropriate X- and Y-lines are each impulsed with half-select current (called read current). Every core that is set at the intersection of these two lines is reset. The pulse is sensed on the corresponding sense winding where it is amplified and used to set a data register latch.

Write

To write into a position, the same X- and Y-drive lines (as in read) are used to select the proper location. However, to write, the current through the lines is in the opposite direction (called write current). Because both of these are half-select currents, they would, unless modified, set all cores in a position. To control which cores are set, another wire (inhibit line) is passed through every core on a plane (Figure ~~2-1-2~~ 7). To prevent setting a core, half-select current is fed on the inhibit line in a direction opposite to the X- and Y-currents. This cancels out half the magnetic force created by the X- and Y-lines and only half-select current passes through a core. In setting a core, no current is applied to the inhibit winding. This permits full-select current to set the core.

Physical Arrangement

The physical arrangement of the cores and the X- and Y-, inhibit, and sense windings of a plane are shown in Figure ~~2-1-3~~. 4

Each X- and Y-drive line goes only through the cores in one row or column. The inhibit winding goes through all cores in an electrical plane, and parallels the X-drive lines. The sense winding is threaded in parallel with the Y-drive lines,

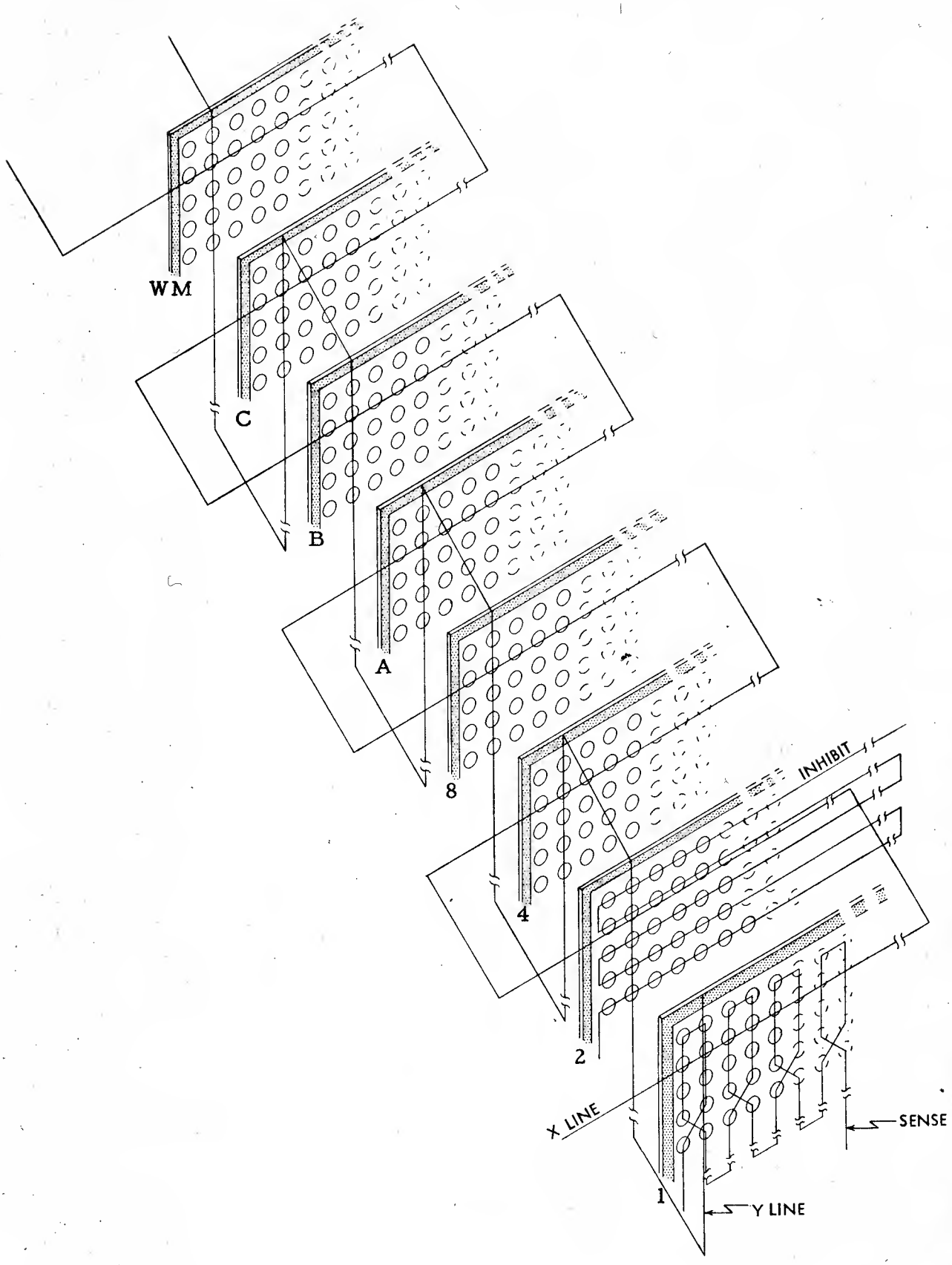


Figure ~~2~~ 7 Core Array Winding

and goes through all cores in an electrical plane. Also the sense winding crosses over at the middle of the plane to cancel the effect of mutual coupling between the lines. In the 1411 core storage, there are actually two inhibit and two sense windings per plane. Thus, for the inhibit and sense functions, the 100-by-100 array is actually two 50-by-100 core planes.

The essential concern is the voltage that is induced in the sense winding as the result of the flux change in the addressed core that is set. The sense winding is crossed at the midpoint of the plane so the Y-drive pulse does not induce enough voltage to be interpreted as a 1, even though the core contains a 0.

For simplicity, Figure 2-4-4 shows the sense winding in electrical plane 1 and the inhibit winding in electrical plane 2. The sense winding of electrical plane 2 is a mirror image of the sense winding in electrical plane 1. The inhibit winding in electrical plane 2 is a mirror image of the inhibit winding in electrical plane 1.

Data Flow Components (Figure 2-4-5)

The data-flow components are:

1. data-register latches
2. inhibit drivers and sense amplifiers
3. logical switching networks.

Because the induced-voltage pulse on the sense line is of low amplitude, a sense amplifier amplifies the pulse to the logic circuit level. It is then used to set a data register latch.

To select the induced pulse from the noise impulses on the sense winding, a short pulse (strobe) gates the sense amplifiers just as the ferrite core reads out.

The data-register latch holds information that is to be again written into the cores. This rewriting of information back into the cores is called regeneration. The time that regeneration occurs is controlled by the inhibit gate and a control line called Storage Regen. This specifies that original information is to be written back into the cores. The data register latch causes the inhibit drivers either to suppress or to allow half-currents to flow in a direction opposing the write currents. Because the write current is in a direction that is opposite to the read current, all cores of an address are set to 1 during the write cycle. The inhibit driver prevents the writing of a 1 by an opposing half current that is under the control of every data-register bit-position that contains a 0.

Storage Cycles

A core-storage unit has two basic types of cycles.

A read-out cycle occurs when information reads out of the ferrite cores and passes on to other units of the system. The information read-out is regenerated (written back into the same cores) during the write portion of the operation.

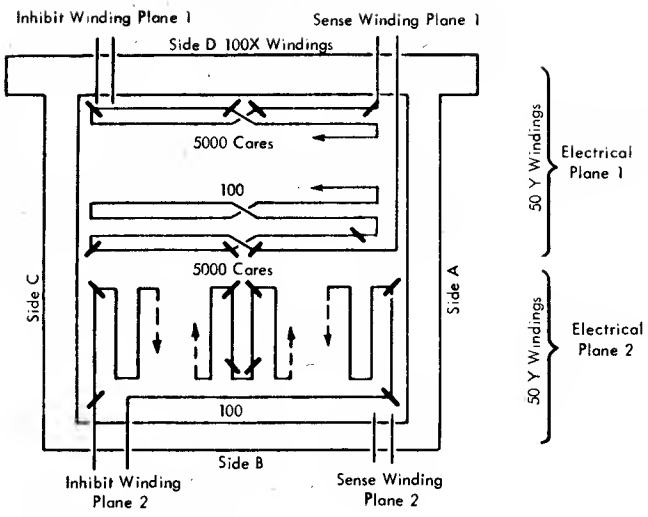


Figure 2-~~1~~ 8 Actual Core Plane

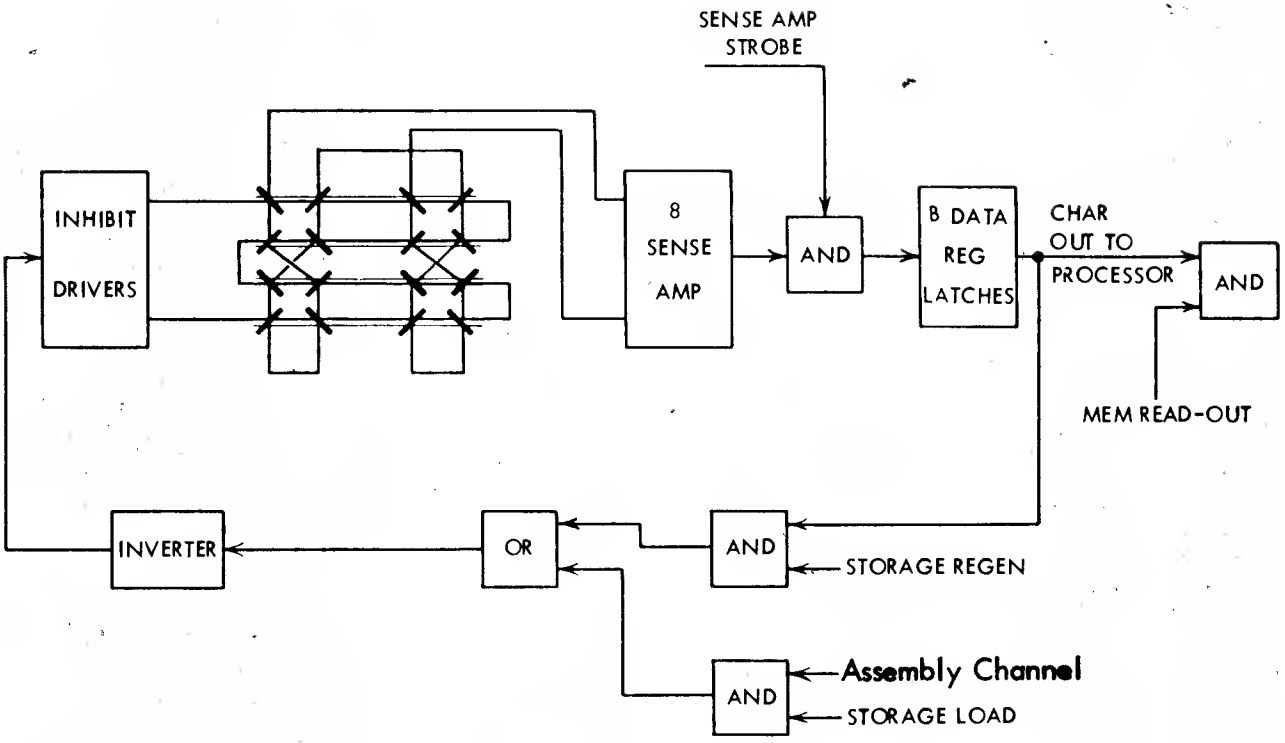


Figure 2-~~1~~3 Care Storage, Data Flow

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A read-in cycle occurs when new information from another unit of the system is to be written into the cores.

The information that is already in the cores reads out to the data register the same as during the read cycle. The write portion of the cycle then writes the new information into the cores. Both read-out and read-in cycles are discussed in the sections entitled Read Out and Read In.

Read Out

To read out of core storage, these steps are necessary:

1. Read the cores in order to set the information in the data latches.

2. Write the information from the data latches back into the cores.

Read. During the first half of any machine cycle (Figure 9) that uses core storage, the same relative core in each plane is pulsed with X- and Y-current in the read direction. This sets all cores at a given address to 0. Any 1's present are picked up on the sense lines, amplified by the sense amplifiers, and used to set the data latches. Cores that contain 0's do not activate any sense lines. The latches associated with these cores remain at 0.

Write. During the last part of any storage cycle (Figure 9) the same X- and Y-drive lines are always impulsed in the opposite, or write, direction. This current pulse is in the direction to place a 1 in the addressed cores. However, if the data-register latches are OFF (0), the inhibit gate pulses the inhibit winding during write time. Because this inhibit pulse is in the direction opposed to the write pulse in the X-winding, the addressed core is pulsed with half-select current that leaves it in the 0-state.

Read-In

To read new information into core storage, three steps are necessary:

1. Read the cores in order to gate information that is already in the cores into the data register.

2. Activate the inhibit drivers (Figure 9) with the new information from some other unit of the system.

3. Write the new information into the cores during the write cycle.

Read. As with every storage cycle, an X- and Y-drive line is pulsed with read current. The sense amplifiers are strobed and the information in the cores is gated to the data latches. The read portion of the cycle thus sets all cores in the addressed location to 0, and also sends the information that was in the cores to the data register.

The new information to be written into storage is gated into the inhibit driver by the storage load signal.

MATRIX SWITCH METHOD OF ADDRESS SELECTION

Load Sharing Matrix Switches (LSMS or matrix switch) are used to select a location in core storage because of their ability to share the required current loads and to reduce the number of driver circuits. The addressing system must select two lines (one X line and one Y line) and supply read and write current to these lines. Since the core array has 100 X and 100Y lines, it is possible to accomplish the necessary selection by having two driver circuits for each X and Y line (one for read and one for write). However, this would require 400 drivers and, obviously, would not be an economical method. By using the LSMS method, the number of drivers needed is reduced to 52: 16 X and 16 Y drivers plus 10X and 10Y power gates. The LSMS can supply currents in both directions: one direction for read and the opposite direction for write.

PHYSICAL PROPERTIES

A matrix switch is made up of ten special pulse transformers housed in a rectangular-shaped heat-dissipating plastic and mounted on a double SMS card.

The core of each transformer is made up of 12 rings of powdered iron (Figure 11), stacked in two paralleled 6-ring cylinders. Each transformer has 16 primary windings and one secondary winding. The 16 primary windings are interconnected, with one set of end windings connected to the 16 matrix switch drivers, and the other set of end windings connected to the power gates (Figure 10). The ten secondary windings are connected to the X or Y drive lines to the core array.

To select one of the 100 X lines to the core array requires ten matrix switches. Each X matrix switch selects one of ten possible outputs by encoding the units position of STAR. The tens position of STAR selects which of the ten matrix switches is used. For example in Figure 13 the heavy black lines show

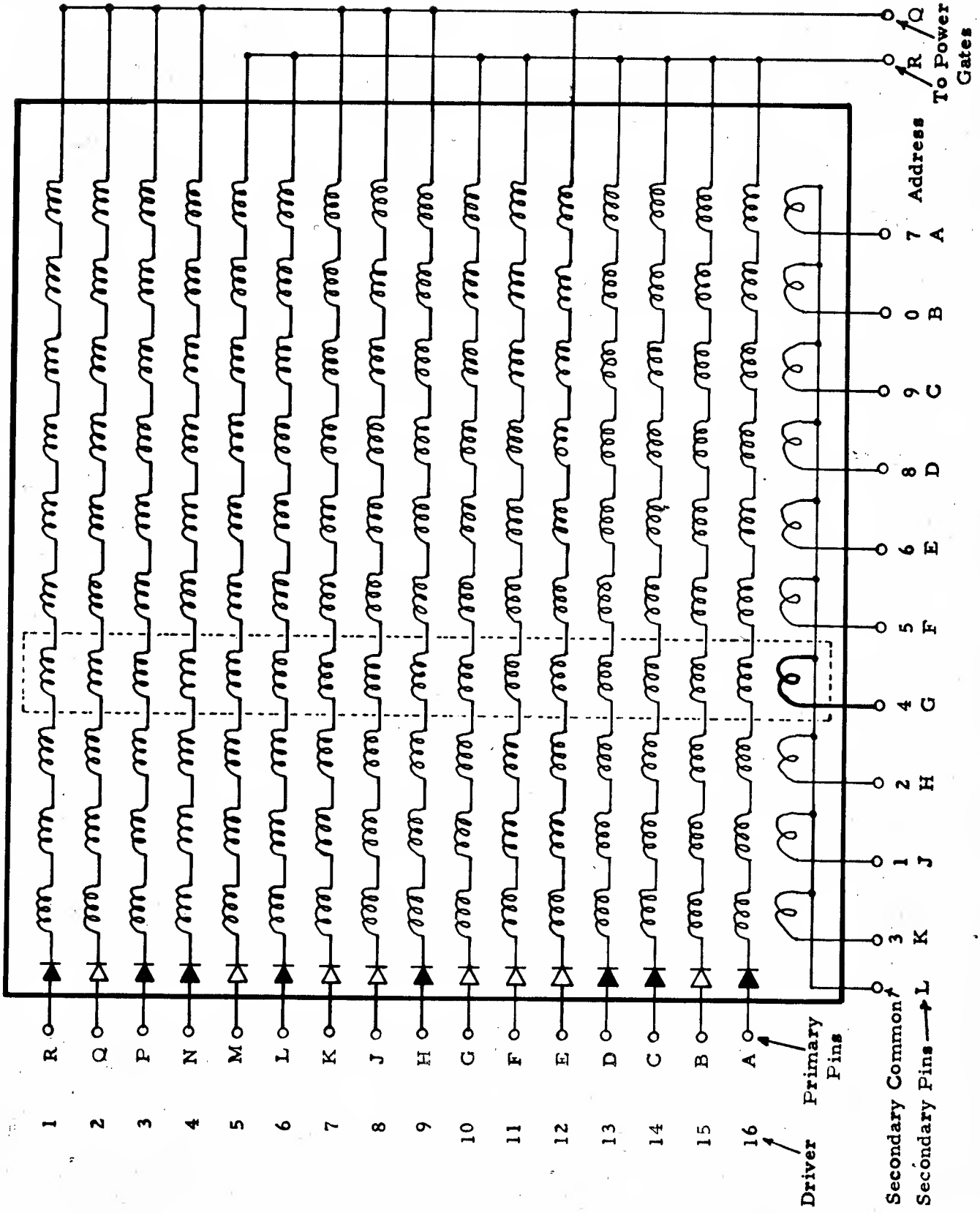


Figure 10 Load Sharing Matrix Switch

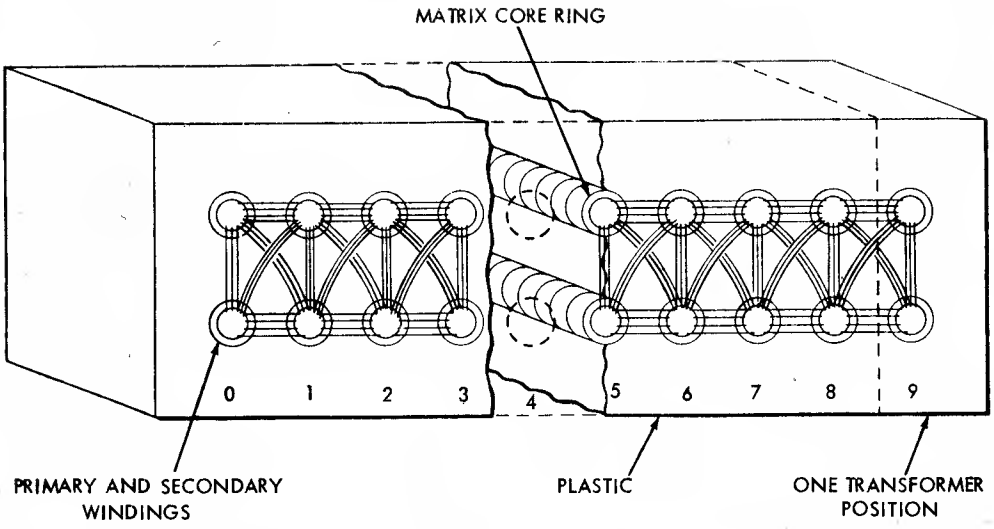
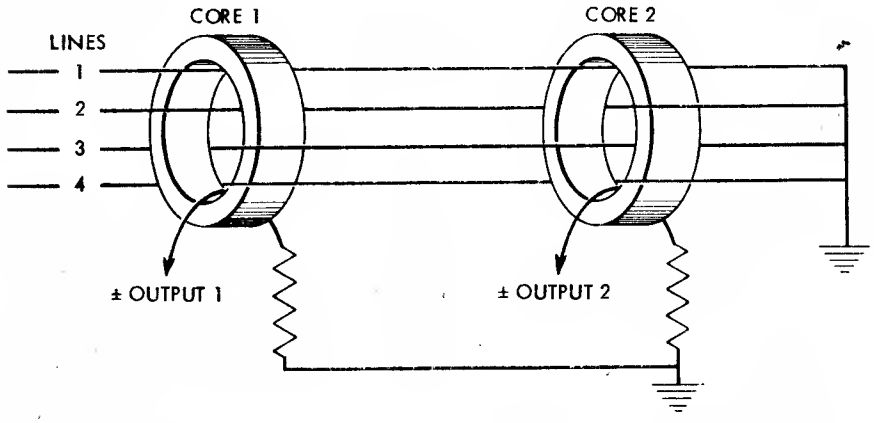


Figure ~~2.1-6~~ 11 Matrix Switch



READ (FORWARD)

MATRIX CORE OUTPUT	ACTIVE LINES			
	1	2	3	4
1	X	X		
2	X		X	

WRITE (REVERSE)

MATRIX CORE OUTPUT	ACTIVE LINES			
	1	2	3	4
1			X	X
2		X		X

Figure ~~2.1-7~~ 12 2 Position-Matrix Switch and Truth Table

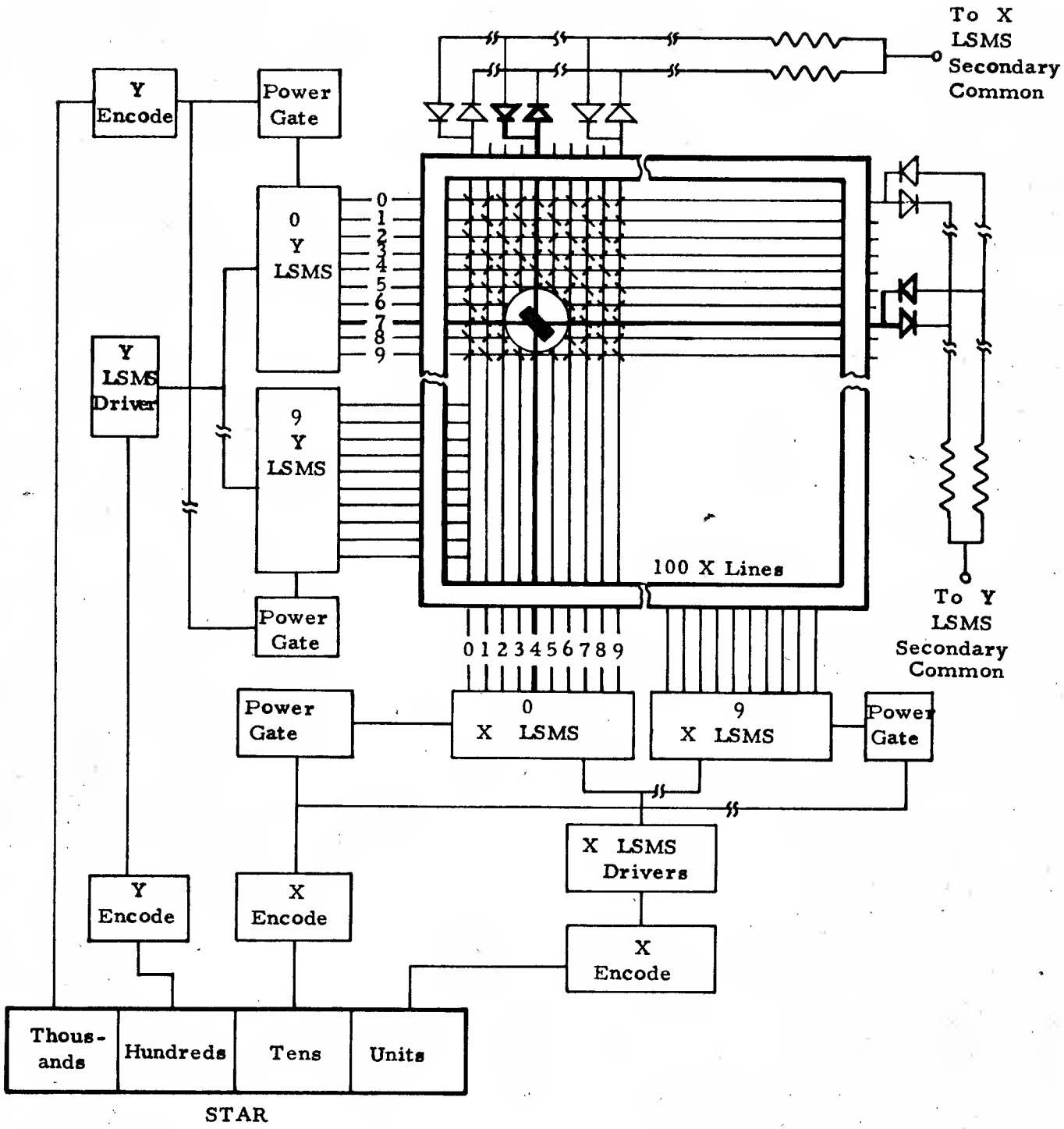


Figure 13 Core Storage Addressing

selection of the address 0704. The units digit, 4, in STAR encodes and drives all ten X matrix switch primary windings in parallel attempting to select the 4 output line of all ten matrix switches. But, because the tens position of STAR encodes and conditions only the 0 matrix switch, the other nine cannot conduct current, and an output is produced only in the desired line, 04. The Y line, 07, is selected by the same method of encoding the hundreds and thousands positions of STAR.

Electrical Properties

The matrix switch winding connections and the pin connections of the double card are shown in Figure 10 . The matrix switch performs two functions: selecting a line, and providing read and write current to that selected line. These two functions are accomplished by the way the windings are placed on the magnetic cores. Each of the ten sections of the matrix switch has its primaries wound so that combinations of the primary currents add or cancel to produce the selecting function. If the pattern of input currents select a particular transformer section, the coincident currents that select it also cause the ferro-magnetic core to flip. Flipping the core sends, by transformer action, a pulse of current on the secondary winding. If the core does not flip, no current appears in the secondary winding.

To cause the matrix switch core to change state, or flip, eight of its 16 primary windings must receive coincident current. During the first part of a memory cycle, or read time, eight windings are pulsed to set the switch core, which produces secondary read current. During the last part of the same memory cycle, or write time, the same switch core is reset to produce write current in the secondary by pulsing the remaining eight primary windings.

For example, in Figure 10 the primary drivers 1, 3, 4, 6, 9, 13, 14, and 16 (black diodes) produce additive primary currents in section 4 and flip the core, sending read current to the core array on the 4 line (secondary pin G). Then during the write portion of the same cycle the remaining eight drivers (2, 5, 7, 8, 10, 11, 12, and 15) flip the core in the reset direction, sending write current on the 4 line.

Figure 14 is a truth table showing the primary combinations necessary to produce each of the ten secondary outputs for read (0) and write (+).

To further explain the operation of the matrix switch, consider the simplified circuit with two outputs and four inputs (Figure 12). With both cores reset, if current passes in the same direction in lines 1 and 2, the flux from each line adds at core 1 to set the core. This induces an impulse in the output winding. As the currents pass through core 2 in opposite directions, there is a cancellation of flux, thus no output. When lines 3 and 4 are impulsed in that same direction, core 1 is reset. This induces an impulse into the output winding in the opposite direction. Again there is no output from core 2. In core 1, lines 1 and 2 are used for forward (read) output. Lines 3 and 4 are used for a reverse (write) output. In core 2, lines 1 and 3 are used for a read output; and lines 2 and 4, for a write output.

Figure 15 shows the circuit details for one matrix switch primary winding, its driver, and the gate circuit. The driver circuit is one of 16 and drives corresponding primary windings in ten matrix switches in parallel. The diode prevents back circuits in an unselected primary winding. The power gate circuit selects which one of the ten groups of windings are permitted to have current flow. Two power gates operate in parallel for each matrix switch for current capacity requirements. The gates are connected to pins R and Q of the matrix switch card (Figure 10).

MATRIX CORE OUTPUTS	ACTIVE LINES DURING READ = 0 WRITE = +															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	+	0	+	0	0	+	0	+	0	0	+	+	+	0	+	0
1	0	0	0	+	+	+	0	+	+	+	0	+	+	0	0	0
2	0	0	+	0	+	+	+	0	+	0	+	+	0	+	0	0
3	0	0	+	+	0	0	+	+	0	+	+	0	+	+	0	0
4	0	+	0	0	+	0	+	+	0	+	+	+	0	0	+	0
5	0	+	0	+	0	+	+	0	+	0	+	0	+	0	+	0
6	0	+	+	0	0	+	0	+	+	+	0	0	0	+	+	0
7	+	+	0	0	0	0	0	0	+	+	+	+	+	+	0	0
8	+	0	0	0	+	0	+	+	+	0	0	0	+	+	+	0
9	+	0	0	+	0	+	+	0	0	+	0	+	0	+	+	0

Figure 14 Truth Table for 10-Position Matrix Switch

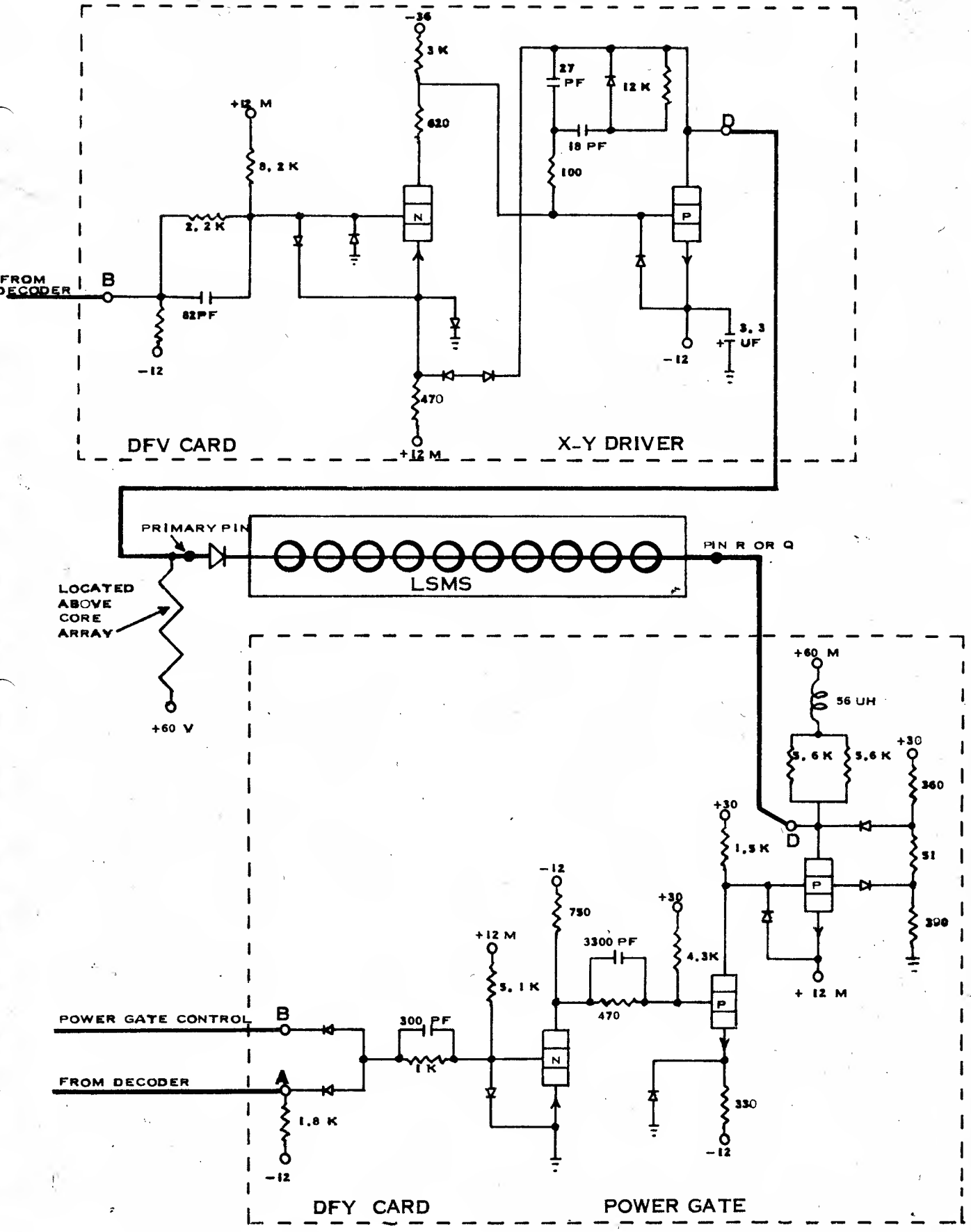


Figure 15 LSMS Driver and Gate Circuits

Noise Problems

Unwanted noise from many sources occurs throughout any core storage unit. The larger the unit, the worse the noise problem becomes.

There is an unavoidable amount of mutual coupling between parallel lines, even with careful spacing and shielding. The cores themselves provide another major source of noise. No core remains completely saturated, and the half-select current tends to move the flux state slightly. The change of the flux state is either toward or away from saturation.

Noise in the sense winding occurs when a core is on the impulsed drive line but is not at the intersection of two drive lines. If all the induced voltages from the half-selected cores were added together, the effect would be troublesome.

One feature that reduces the half-select noise problem is the staggering of read pulses. By energizing one drive line (Y - drive line) in advance of the other (X - drive line), the number of half-selected cores at a given time is reduced. This reduces noise. Later in the cycle, when the X-drive line energizes, and the sense-winding output is used, the noise from the half-selected cores on the earlier Y-drive line has subsided. This delayed read pulse reduces the noise problem.

A second method of noise reduction results from physical arrangement of the windings of the core plane. Cores, drive windings, and sense windings are so arranged that one-half of the half-selected cores tend to cancel the noise induced by the other half of the half-selected cores of a plane.

CORE STORAGE ADDRESSING

The 1411 core storage unit reads in or reads out a single character during a 4.5-microsecond cycle. Reliability is insured by parity checking all information read into or out of the core-storage unit.

The addressing layout including character selection, inhibit logic, and the clock logic is shown in Figure 16 for a 40K model.

The 40K core array requires 40,000 valid five-position addresses from 0,000 to 39,999. The address is read from the CPU into the storage address register (STAR). The STAR stores the address while its output is encoded in order to select the proper character to read out.

Operation

Figure ~~2.1-11~~ 17 shows the locations of the addresses in storage and the encoding that is necessary to select the X- and Y-lines. When the address is read into the STAR, the units and tens positions are encoded to drive and to gate the ten load-sharing matrix switches (LSMS) that select the X-line. The hundreds and thousands positions of STAR are encoded to drive and to gate the ten matrix switches that select the Y-line. The coincidence of these two lines causes four characters to be read out of cores into the four B-data registers. The ten-thousands position of STAR is fed to the character-selection circuits that determine the character to be addressed. The output of character selection is fed to Character Regen or Load where is combines with either Memory Regen (read operations) or Memory Load (write operations) to control which characters are regenerated, read out of storage, or loaded into cores from the assembly area. If Memory Regen is up, all character regen lines are brought up to reread the characters into cores. Also a character-select line is brought up to gate the desired B-data register onto the B-channel. When Memory Load is up the character that is position-selected is loaded from the assembly area, while the other three characters are regenerated.

10K Core Array

Figure ~~2.1-12~~ 18 shows the locations of the addresses in a 10K storage unit and the encoding that is required to select the proper character. When the address is read into STAR, the units and tens position of STAR are encoded to drive and to gate the ten matrix switches which select the X-line. The hundreds and thousands positions of STAR select the Y-line. The coincidence of the X- and Y-lines causes two characters to be read out into the two B-data registers. The thousands posi-

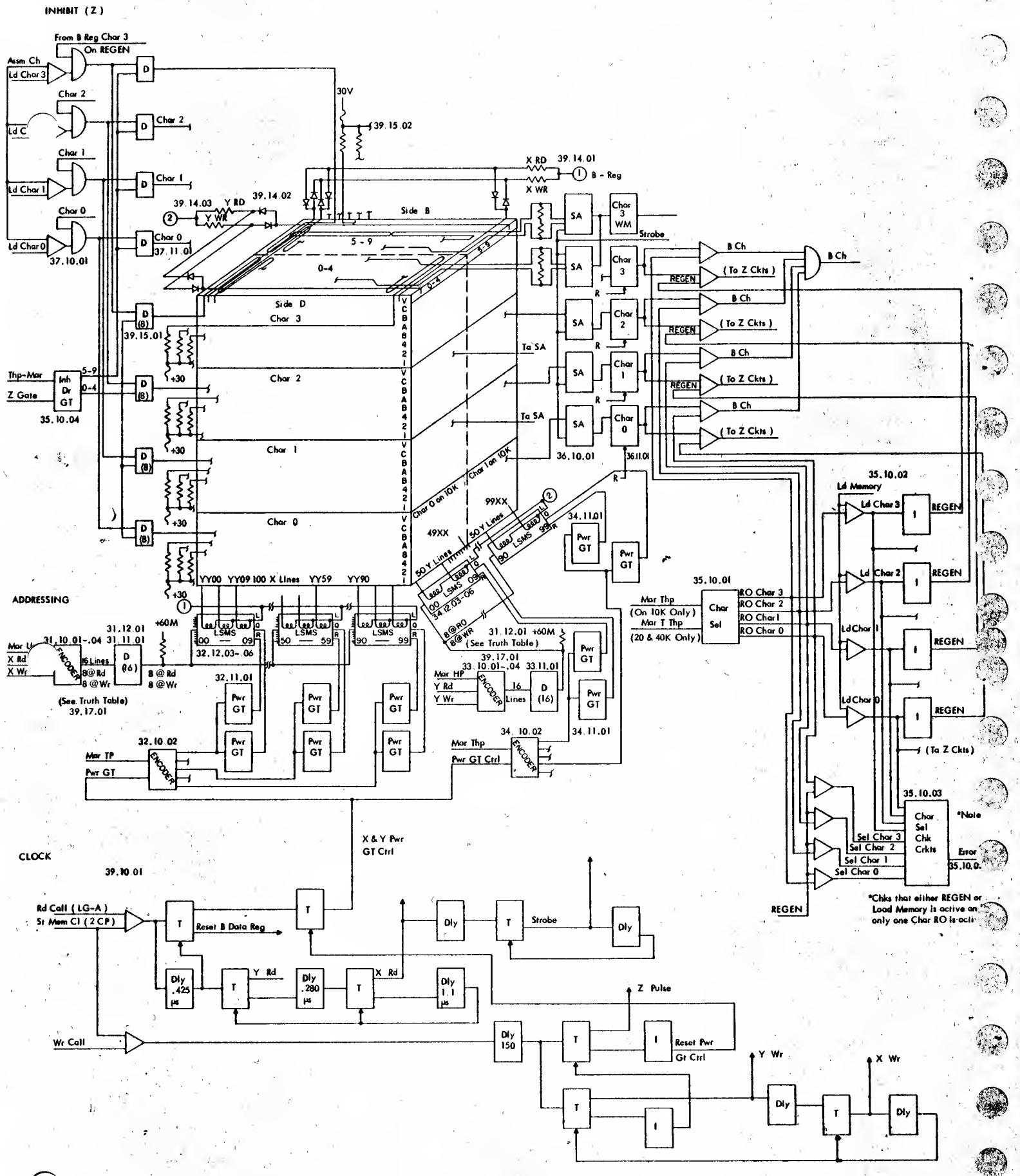


Figure 16 1410 Core Storage

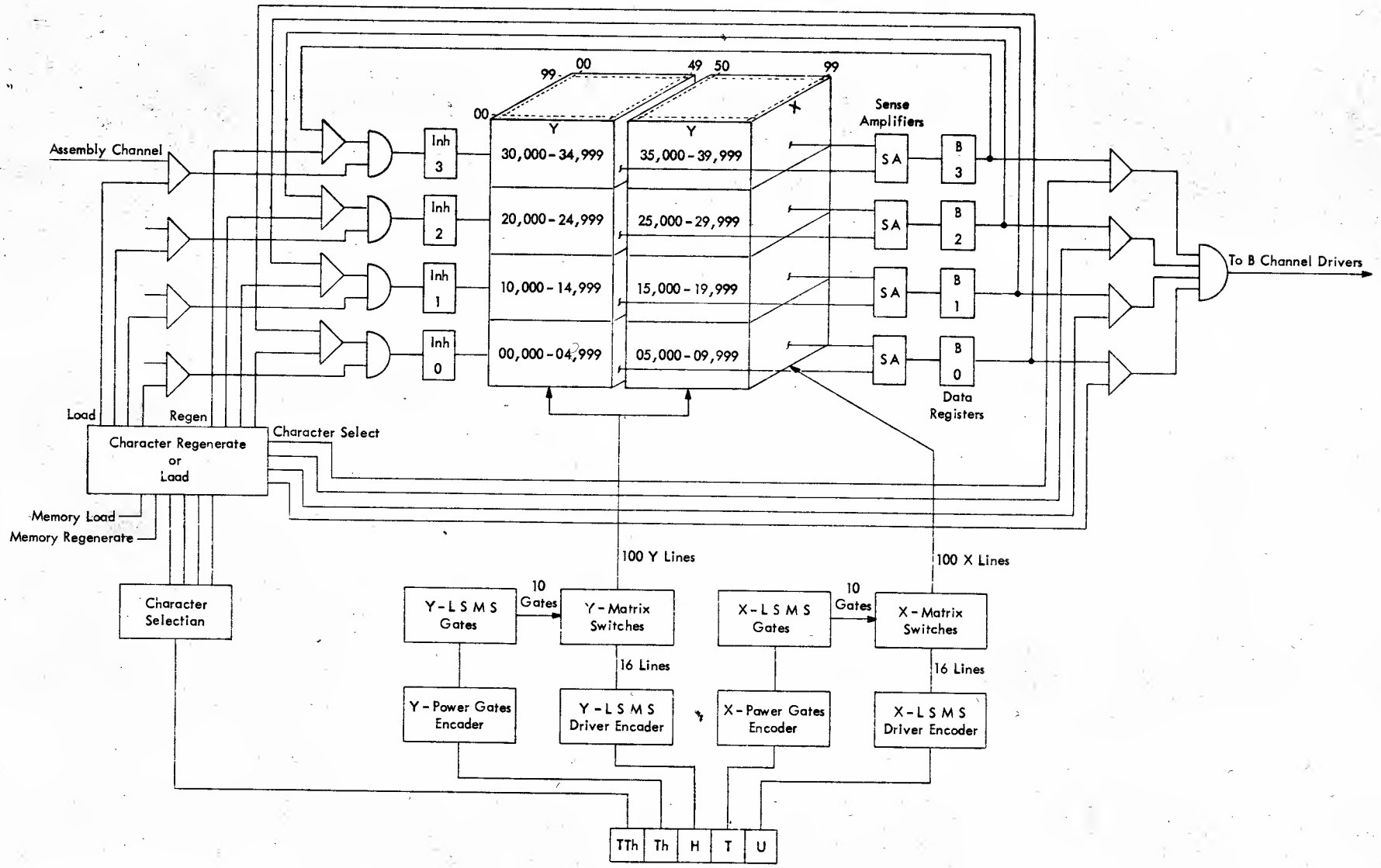


Figure 2-1-11 40K Core Storage Addressing

17

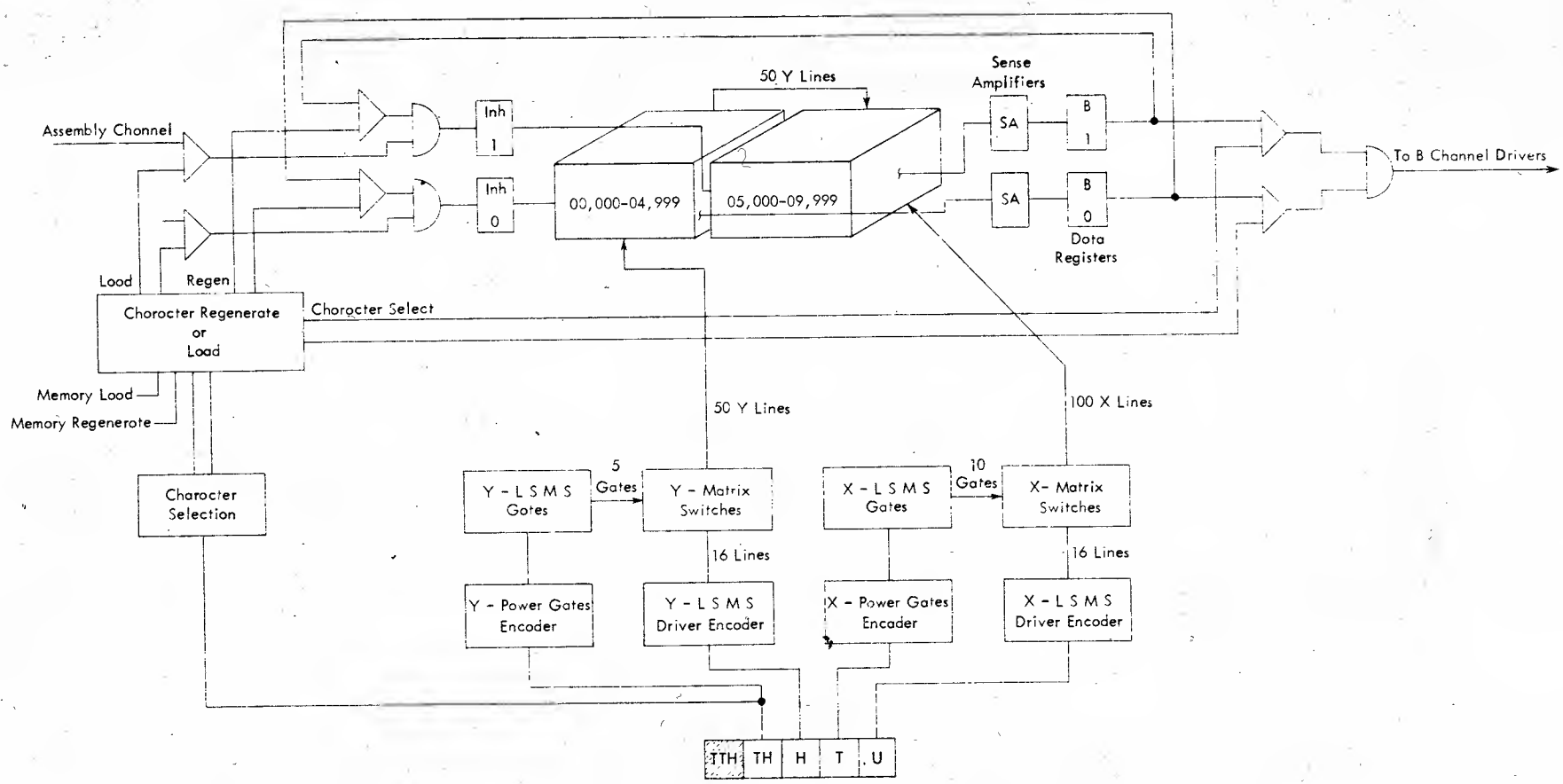


Figure ~~2.1-12~~ 18 10K Core Storage Addressing

tion of STAR is fed to the character select where it combines with Load Memory or Memory Regen to gate the character into or out of storage.

MEMORY CLOCK

Every storage cycle, regardless of CPU operation, has a read and write time. On a read-out operation, the write time is used to regenerate the data into the cores. On a write operation, the cores are read out to clear the position where the new character is to be read in.

The memory clock provides the read and write pulses that are required by the storage unit.

Read

The CPU initiates a storage cycle with a read call that, along with Start Memory Clock, resets the B-data registers, activates the X- and Y-power-gate controls, and initiates a .425 μs delay (Figure ~~2-1-13~~ 17).

The X- and Y-power-gate control lines combine with the output of the X- and Y-power gates encoder to drive the X- and Y-LSMS gates. After the .425 μs delay, the Y Rd line gates the hundreds position of STAR to the Y-matrix-switch driver encoder that, along with the matrix-switch gates, drives the selected Y-line.

Y Rd also activates a .280 μs delay that initiates the X Rd to gate the X-line-drive.

The X Rd line impulses two more delays. One delay, of .725 μs, initiates Strobe that controls the sense amplifiers. The other delay of 1.100 μs, drops the X Rd and Y Rd lines to complete the read-out of cores.

Strobe also initiates a .350 μs delay to drop itself. Figure ~~2-1-14~~ 20 is a timing chart for a storage cycle.

Write

A write call from the CPU initiates the write portion of the storage cycle. When the memory clock receives a write call, it combines with Start Memory Clock to impulse a .15 μs delay. The .15 μs delay initiates a Z-pulse that gates the inhibit drivers. The .15 μs delay also brings up Y Wr. This again gates the hundreds position of STAR to the Y-matrix-switch encoder to control the selection of the proper Y-line. Y Wr also impulses a .28 μs delay that initiates X Wr to select the proper X- line.

All the conditions are now present either to regenerate or to write a new character into the cores.

X Wr also impulses a 1.2 μs delay which drops the X- and Y-write lines. When Y-write drops, it turns off the Z-pulse. This in turn drops the X- and Y-power gate controls.

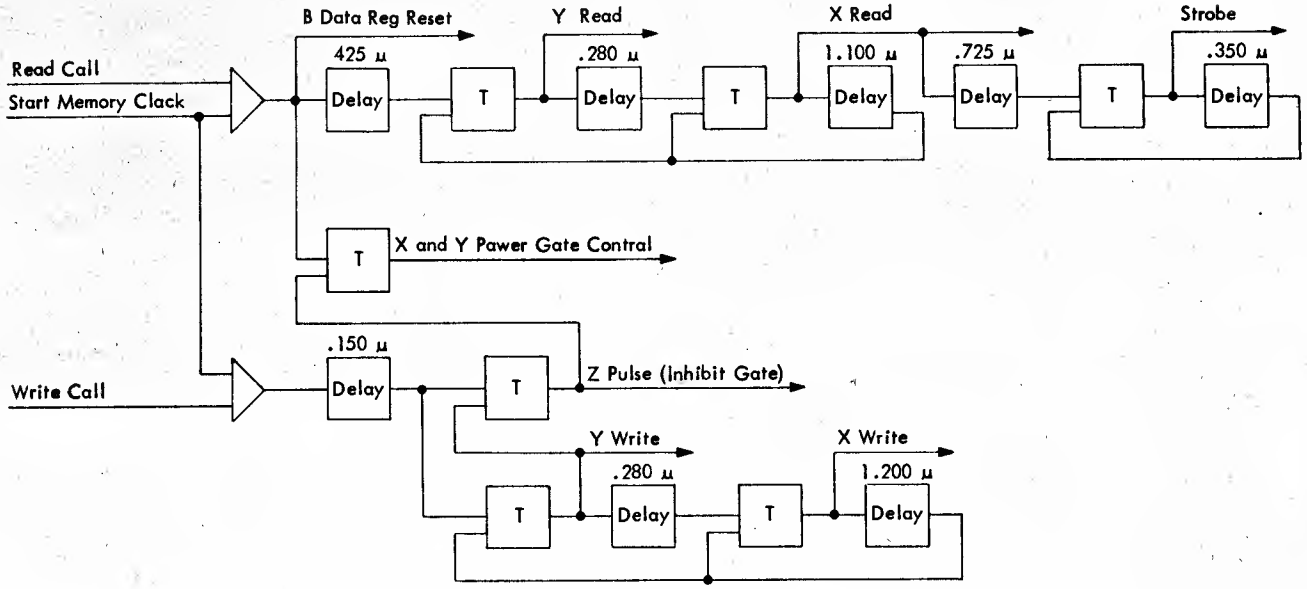
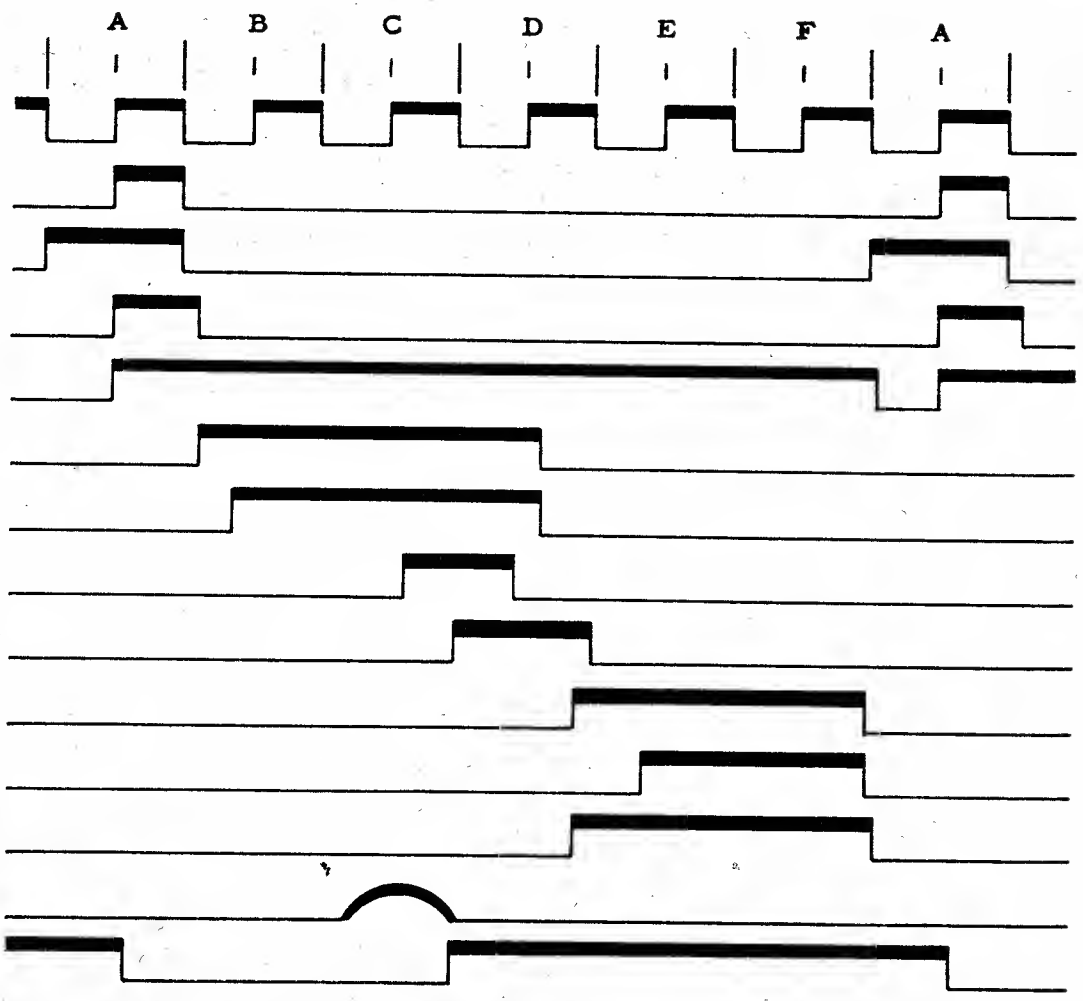


Figure 2~~-1-13~~ Storage Clock

19



	Logic Gates	
1	Start Mem Clock	14.71.51
2	Set STAR Gated	14.17.16
3	Read Call	11.10.32
4	B Data Reg Reset	39.10.01
5	X & Y Pwr Gate Ctrl	39.10.03
6	Y Read	39.10.01
7	X Read	39.10.01
8	Sense Strobe	39.10.03
9	Write Call	12.12.31
10	Y Write	39.10.02
11	X Write	39.10.02
12	Z Pulse (Inhibit)	39.10.02
13	Sense Line	36.10.01
14	Data Out	36.12.01

Figure 20 Memory Cycle Timings

Length of Storage Cycles

A storage cycle in which all characters are to be regenerated can be completed in 4.5 μs or six logic-gate pulses. In this case, the write portion of the storage cycle starts at logic-gate D with the write call from the CPU.

On operations where a character is read out of storage to be combined with another character before it is read back into cores, the storage cycle is increased in length in order to allow the CPU time to construct the new character. In this case the write call is delayed to a later logic gate pulse.

B-Data Register Set Check

The B-data register set check insures that the correct core-storage operation occurs. The circuit makes certain that on every storage cycle the B-data register receives an impulse to reset it.

Some of the failures this check recognizes are:

1. Failure to start the storage clock.

   a. If the memory clock does not start, the last character that was read out of the B-data register again reads out. Without this check, the error would not be caught. It is caught because the memory clock must start to develop the reset pulse.

2. Failure to receive X- or Y-line current or strobe pulse.

   a. If the B-data register is reset and no new data is read in, the B-channel validity-check circuit detects the error.

The circuit for the check is on logic 18.14.06. Both triggers are reset OFF. One trigger changes status on the fifth logic gate pulse of every storage cycle. The other trigger changes status on every B-data register reset pulse. As long as both triggers remain in the same condition (ON or OFF), no error is indicated. If the one trigger fails to receive a B-data register reset pulse, the triggers become opposite in status. The outputs of the triggers then cause a B-data register reset error. This stops the machine and lights the B-data register set-check indicator.

Character Gating

On a 20K or 40K core-storage unit, the ten-thousands position of STAR is fed to character selection (35.10.01) where the bit configuration brings up either RO character 0, 1, 2, or 3. RO character 0, 1, 2, or 3 combines with load or regenerate memory to select, or load that character (35.10.02). All characters are controlled to regenerate except a character that is to be loaded from the assembly area.

On a 10K machine, the thousands position of STAR is fed to character selection where the bit configuration for characters 0 through 4 brings up RO character 0, and 5 through 9 bring up RO character 1.

B-Character Select Check

The addition of a B-character select check circuit increases the reliability of the core-storage unit. This circuit insures that one, and only one, character is either gated out to the B-channel or read in from the assembly unit.

Operation

On a 40K storage unit there are eight character-control lines: four character-select, and four character-load. These eight lines combine (35.10.03) to bring up one of the two character-select error-check lines. If more than one character-control line is up, both of these character-select error check-lines are brought up to indicate an error condition. If none of the character control lines are up, both of the character-select error-check lines are down. This is also recognized as an error condition.

This operation check detects errors in programming that cause invalid addresses. Examples: 40,000-and-above on a 40K core array; 20,000-and-above on a 20K core array. On a 10K core array, invalid addresses are detected by the address-bus validity check.

7251 MODEL 1 ADDITIONAL 60K MEMORY

The IBM 7251 Model 1 Additional 60K Memory is an optional feature that provides the 1410 System with a total of 100,000 positions of storage. This feature is installed instead of the 1411 Model 5 that provides a maximum of 80,000 positions.

The 7251 requires the installation of an additional standard rack and panel module designated Module Z. (Figure 1). Component layout in this module is similar to the standard Module B and the standard Module Z of the 1411 Models 4 or 5 (60 or 80 K).

LOGIC FLOW

Logically the 7251 permits the 1411 to operate with one increased capacity storage unit. The addressing method is changed only to make all locations up to 99,999 valid addresses. Although there are two physically separate core arrays, the logical operation is one single storage unit. This is accomplished by causing both arrays to operate on every storage cycle which reads out ten characters into ten B data registers. The ten thousands position of STAR selects one of the ten characters the same way that one of four characters is selected in a 40K model.

Because the two separate core arrays must function as one storage unit, they must be timed to operate in parallel. The arrays are synchronized by a common clock. The memory clock that supplies the X-Y read and write gates and inhibit gate for the Module B also supplies the same pulses to the Module Z. However, the strobe pulses for the sense amplifiers for the two arrays have separate delay circuits. Generating the strobes separately permits setting each timing to its optimum value. See Figures 21 and 22.

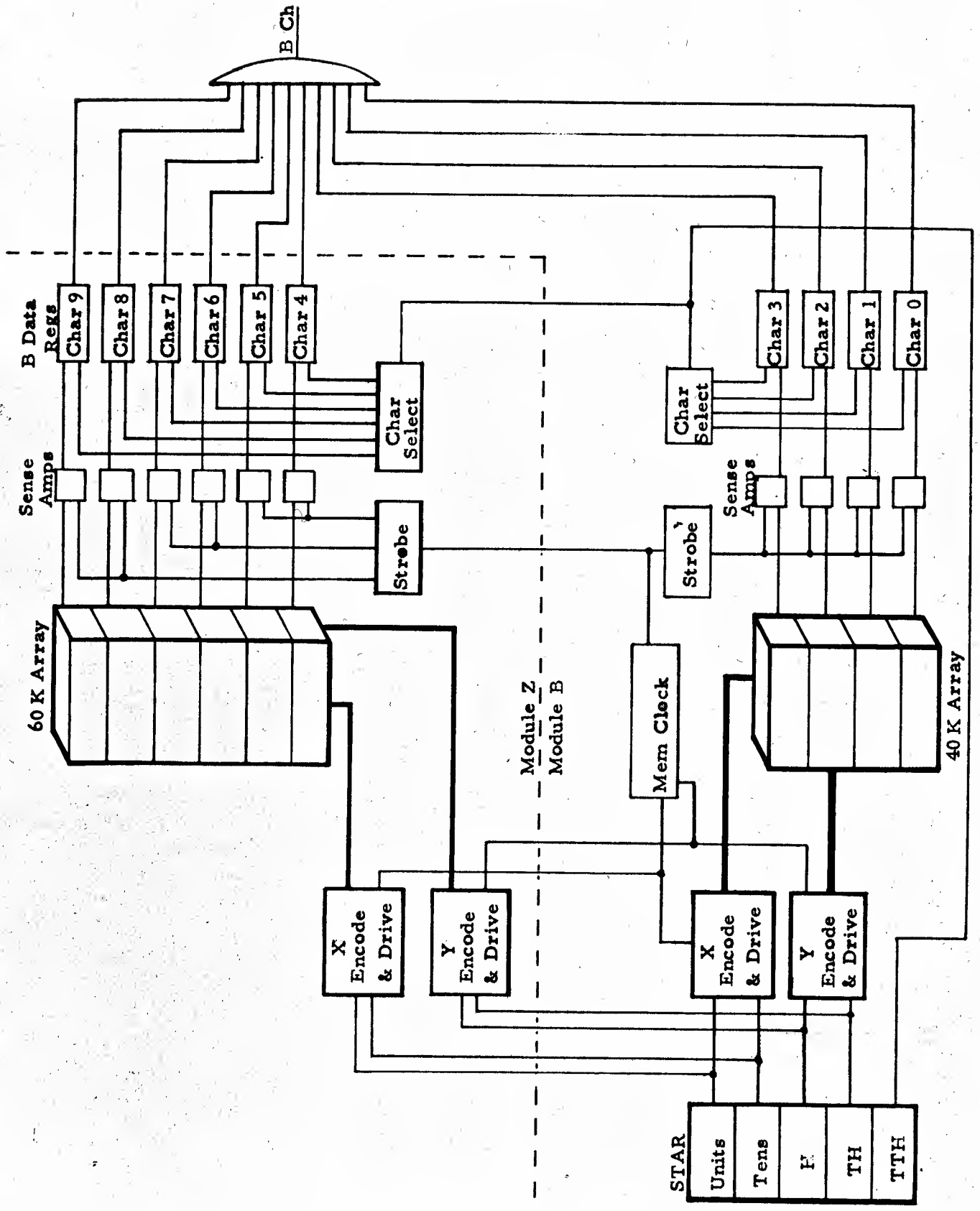


Figure 21 7251 Model 1 Read Out Data Flow

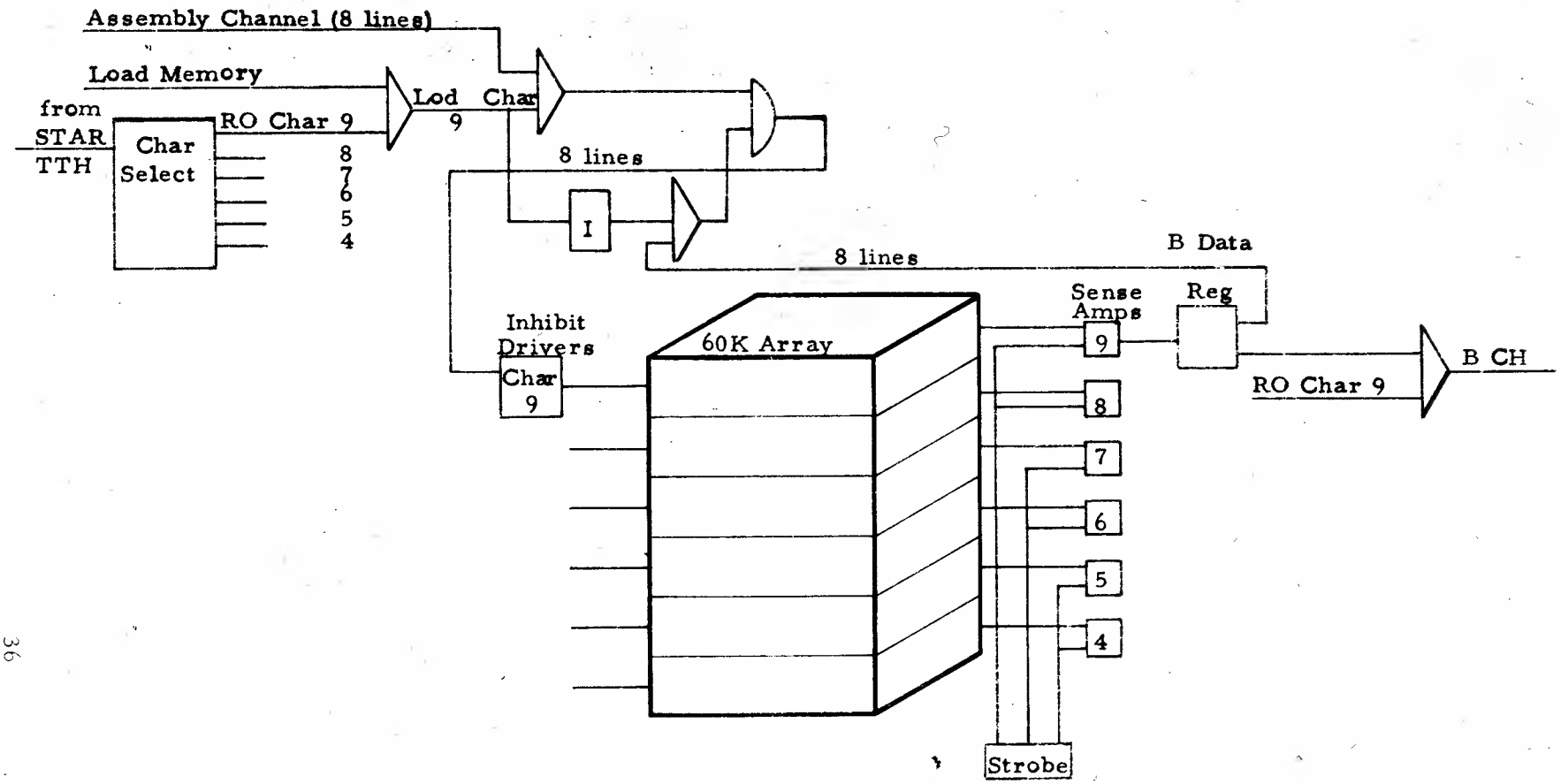


Figure 22 7251 Model 1 Regen and Read In Data Flow

ADDRESSING

The addressing circuits in the 7251 Model 1 are duplicates of the circuits found in the Module B of the 40K capacity 1411. The Matrix switches, the LSMS Drivers, the LSMS gates, and the encoding power gates are the same components and serve the same logical functions (Figure 23). Outputs of the Storage Address Register (STAR) have added driver circuits to supply the additional loads of the Z module.

POWER SUPPLIES

The 7251 Model 1 gets 208 V AC from the A module of the 1411. All the DC voltages needed in the Z module are developed by power supplies mounted in the Z module. These DC voltages are:

+60M
+30M
+12
-12
-6
-36
+30

These power supplies are located in the panel 2 position of the Z module (Figure 24). Also, because of space requirements, power supplies are mounted on a hinged gate on the card side of panel 4 (Figure 25).

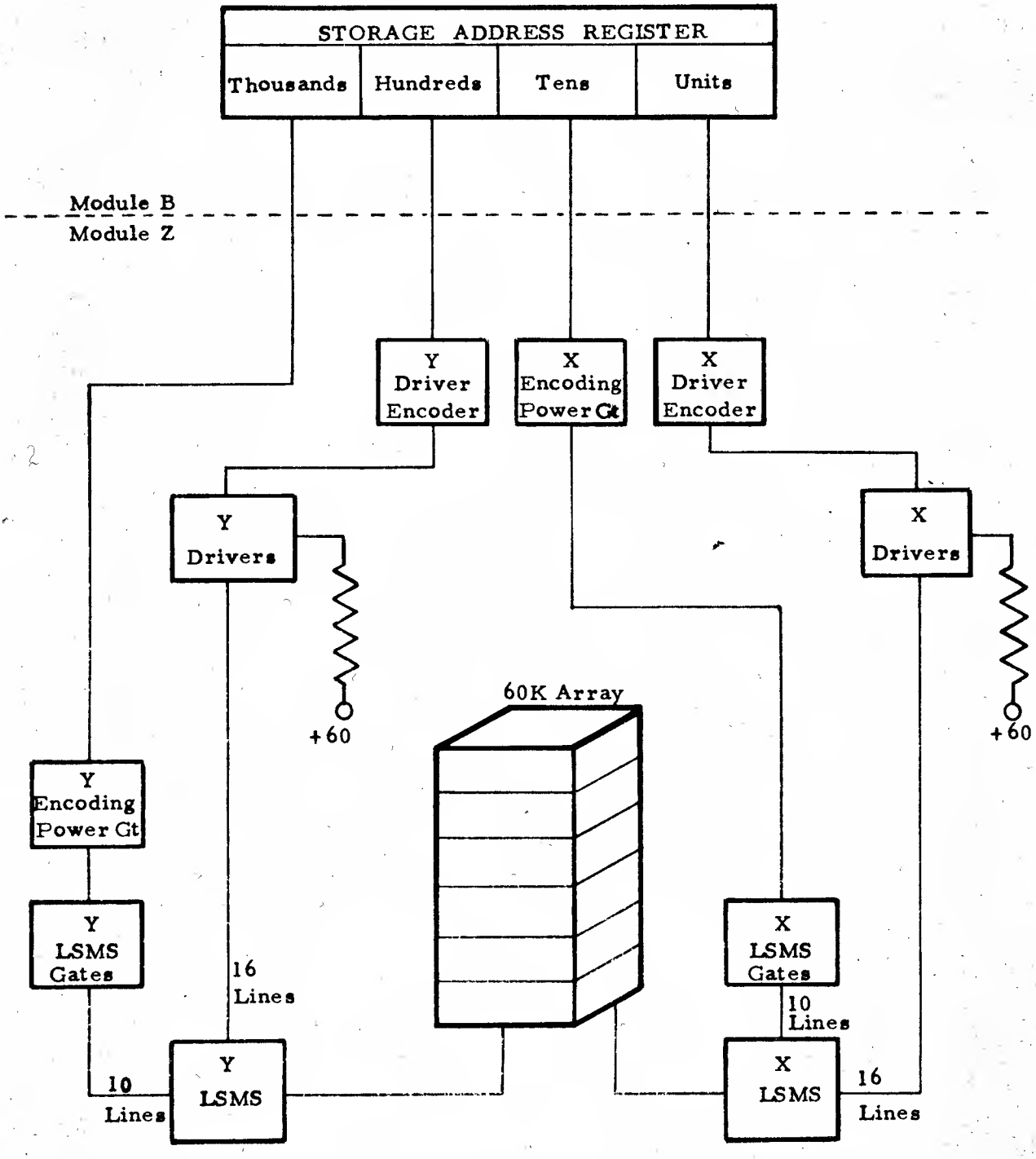


Figure 23 X Y Decoding

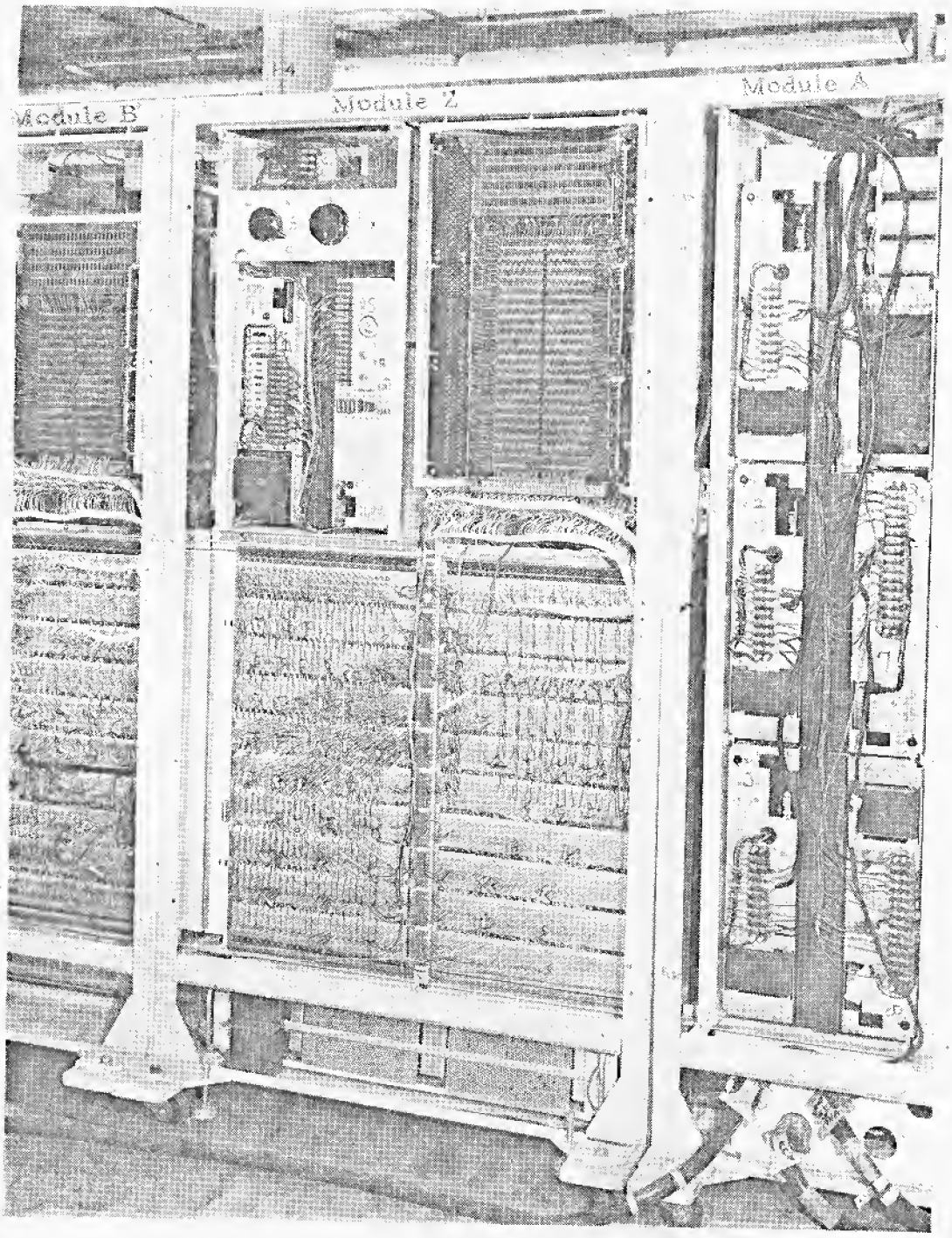


Figure 24 7251 Model 1 Wiring Side

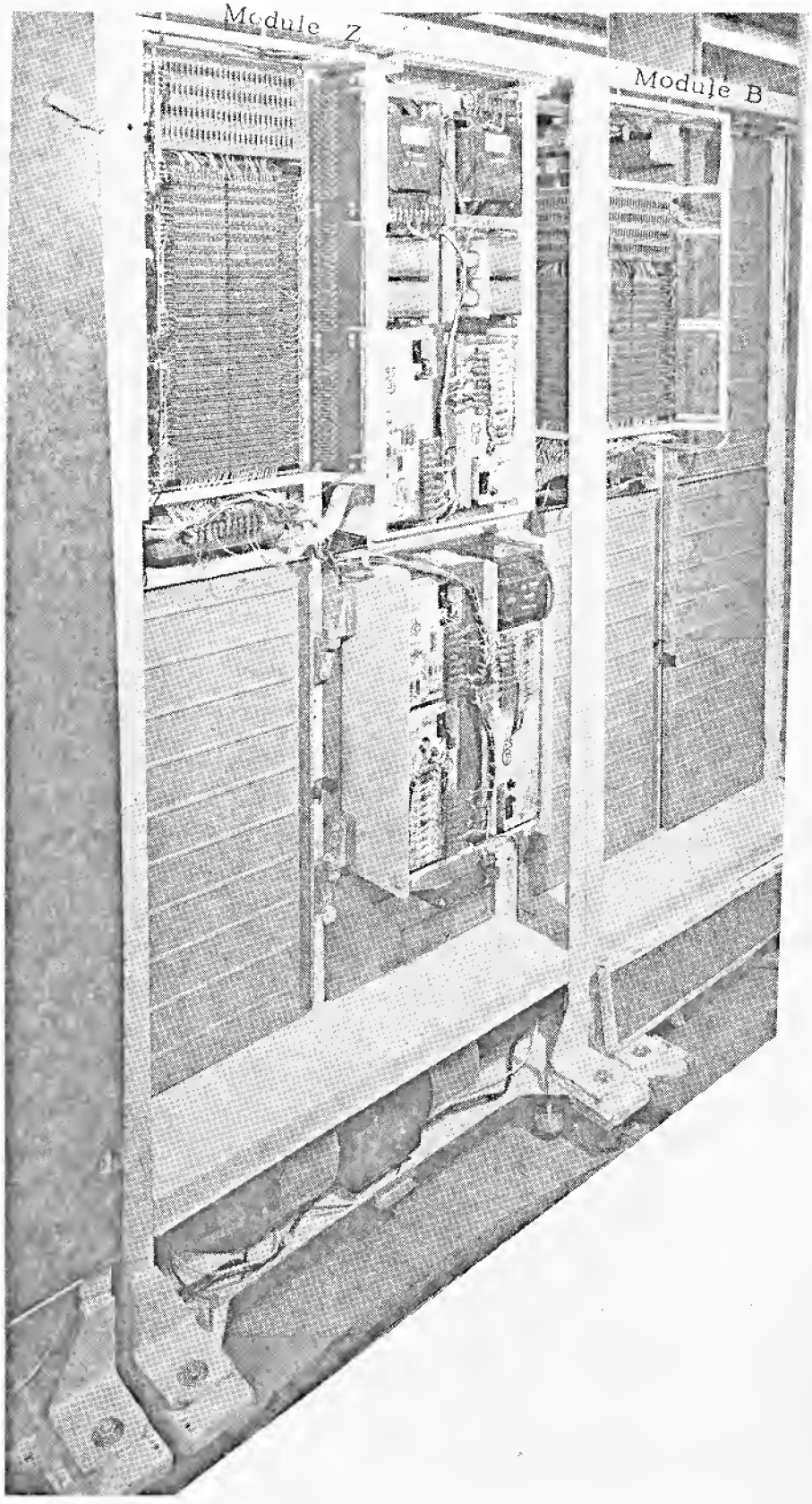


Figure 25 7251 Model 1 Card Side

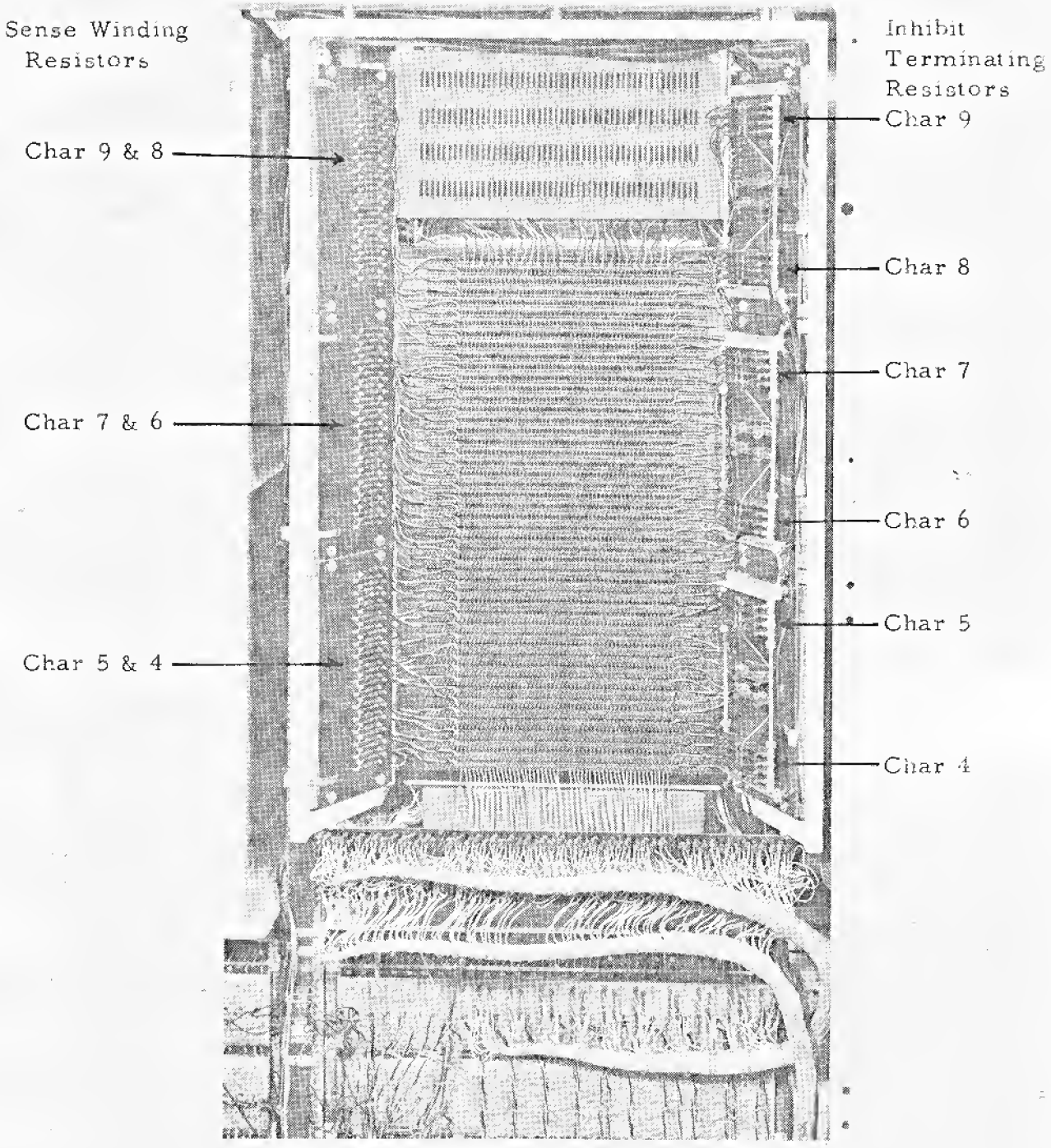


Figure 26 60 K Array

MODELS 4 AND 5

The core storage of the 1411 models 4 and 5 provides additional storage capacities of 20,000 and 40,000positions, for totals of 60,000 and 80,000. These two models require the module Z to be added between modules A and B (Figure 1).

The additional core array is mounted in the module Z and is identical to the 20,000 or 40,000 position capacity module B. The model 4 or 5 thus contains two physically separate core arrays, but they operate as one logical storage unit.

The only difference from the operator's or programmer's viewpoint is that the addresses from 40,000 through 79,000 (80K model 5) are available for use in addition to 00000 through 39,000 (40K model 3). Overflow, wraparound, or indexing from one array to the other requires no special consideration, the two arrays are one larger capacity storage unit.

Addressing

Because the two core arrays are physically the same, the addressing circuits are also alike. The same matrix switches, power gates, encoders, sense amplifiers, and inhibit drivers used in the module B are duplicated in the module Z. The module Z has a separate clock exactly like the standard clock shown in Figure 19.

The address in STAR is sent to both storage units. Because of the added line length needed to take the signals to the module Z, powering circuits are added to the STAR outputs. Both encoders decode the address but only one of the clocks is permitted to start on a given memory cycle. Selection of one of the two clocks is performed by the ten thousands digit of STAR. If the the ten thousands digit of STAR contains a 4 bit, the clock in module Z starts and cycles the additional storage unit. If no 4 bit is present, the module Z array is not started. Instead the module B array is used. (Figure 27).

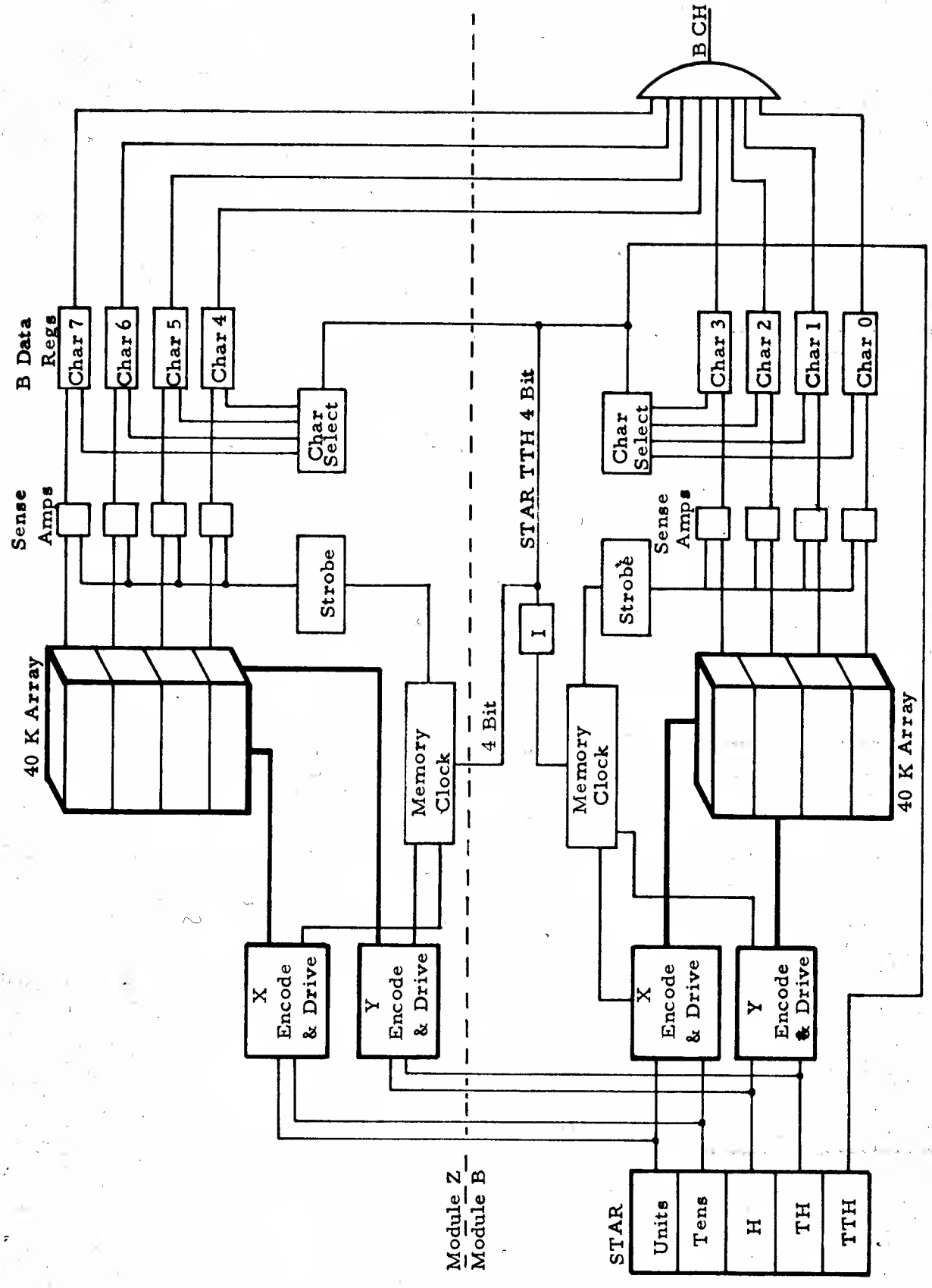


Figure 27 1411 Model 5 Data Flow

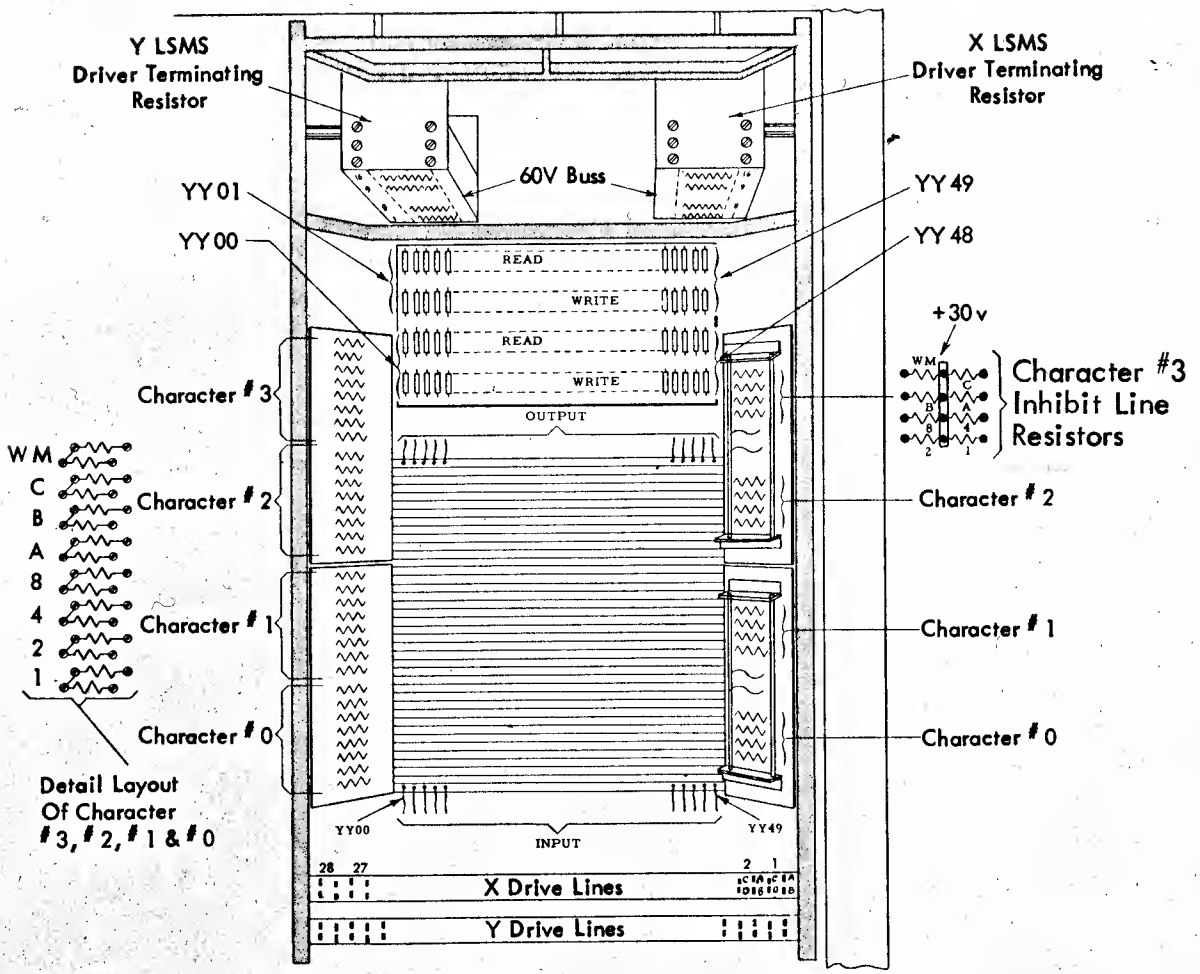


Figure 28. Side D of Core Storage—View from Front of CPU

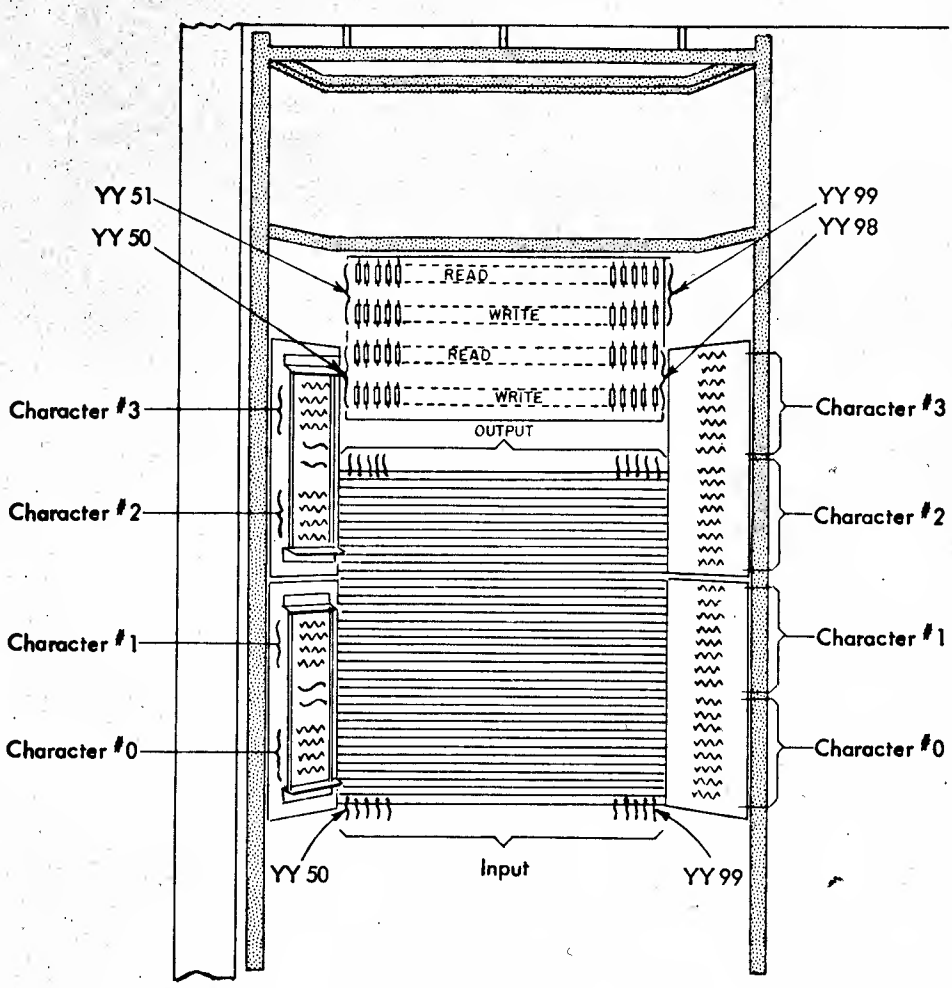


Figure 1~~2~~7. Side B of Core Storage—View from Back of CPU

29

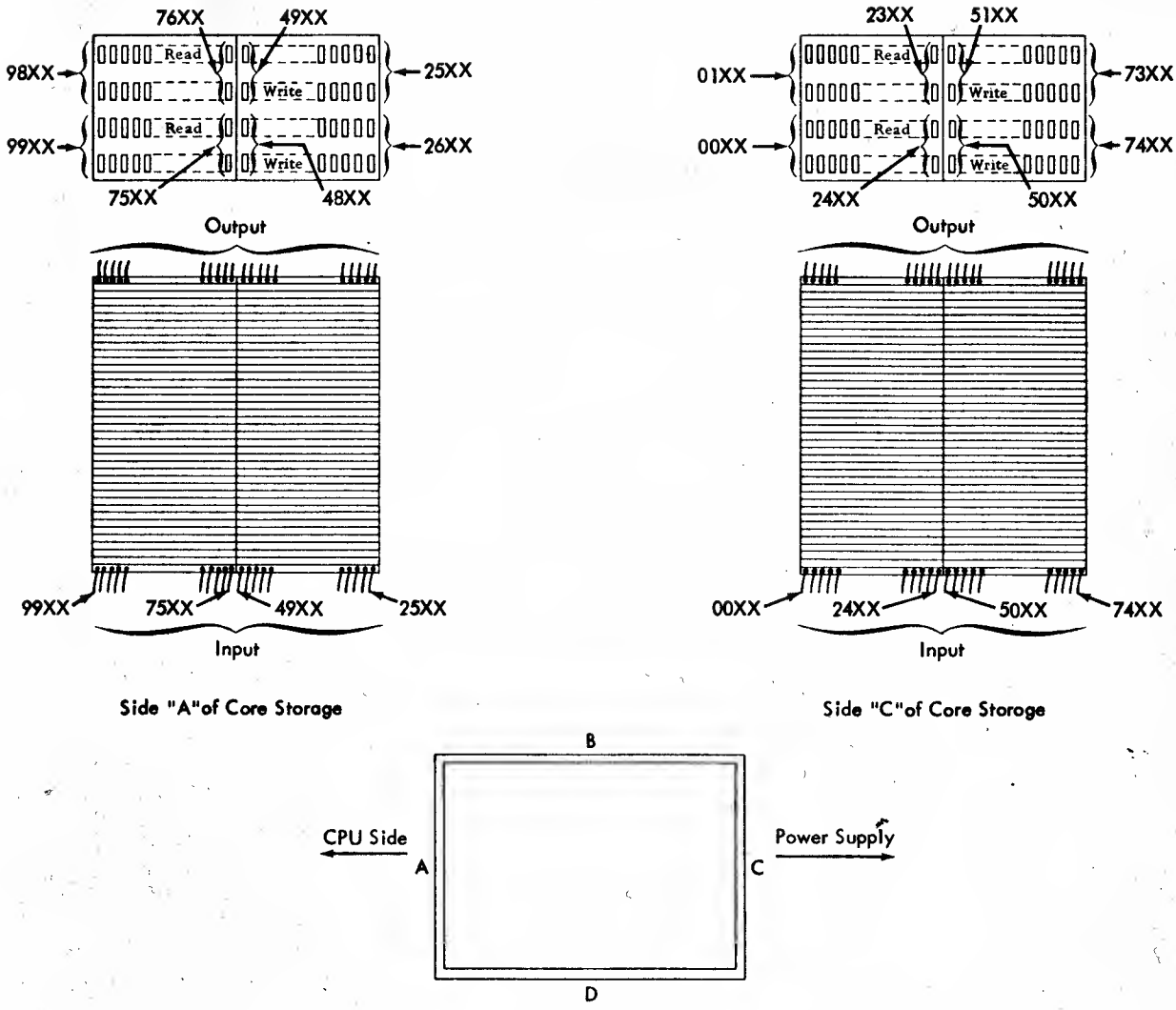


Figure 12-8. Sides A and C of Core Storage—Views from Top and Sides

30

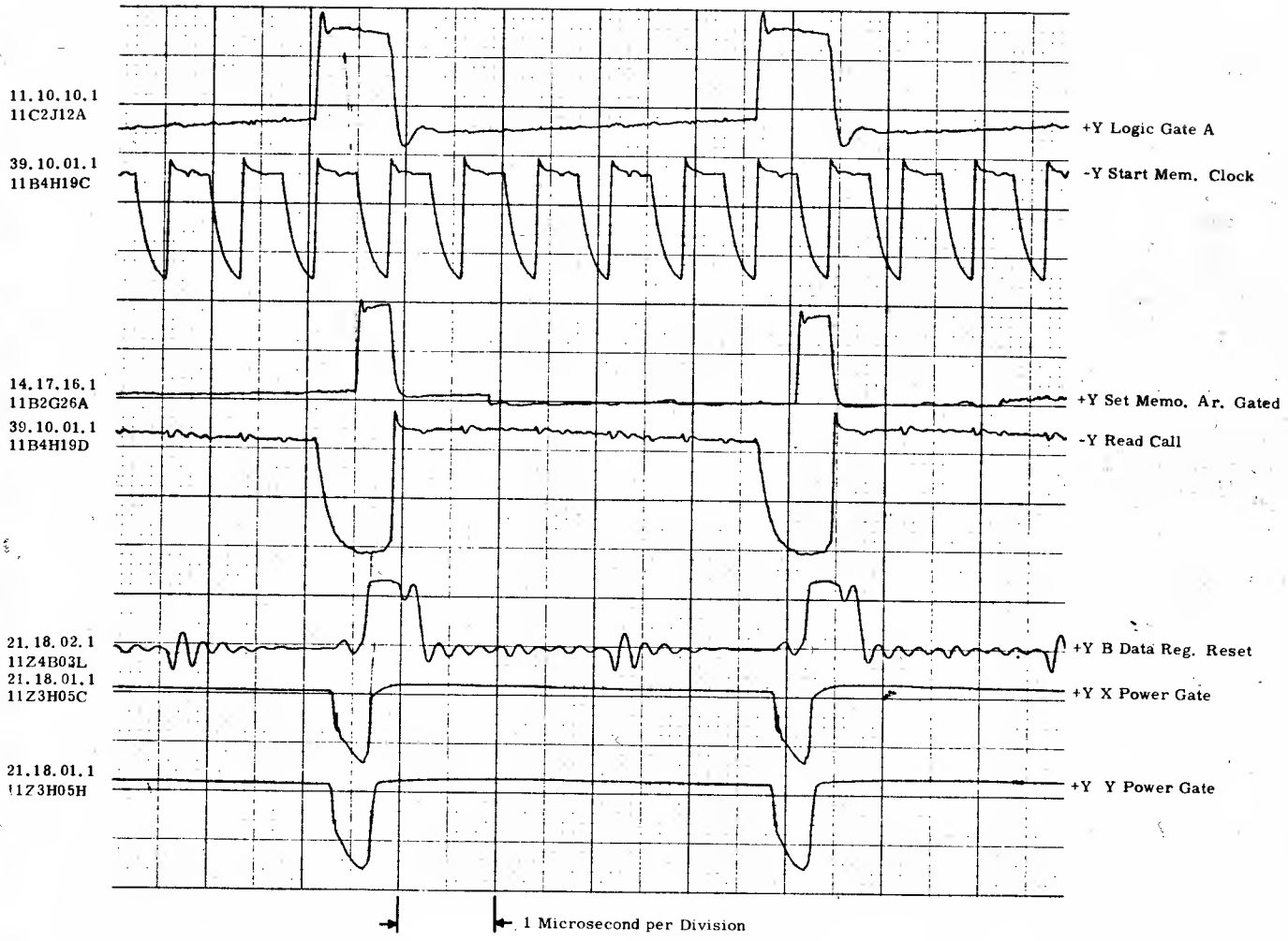


FIGURE 31-A Additional 60K Memory Timings

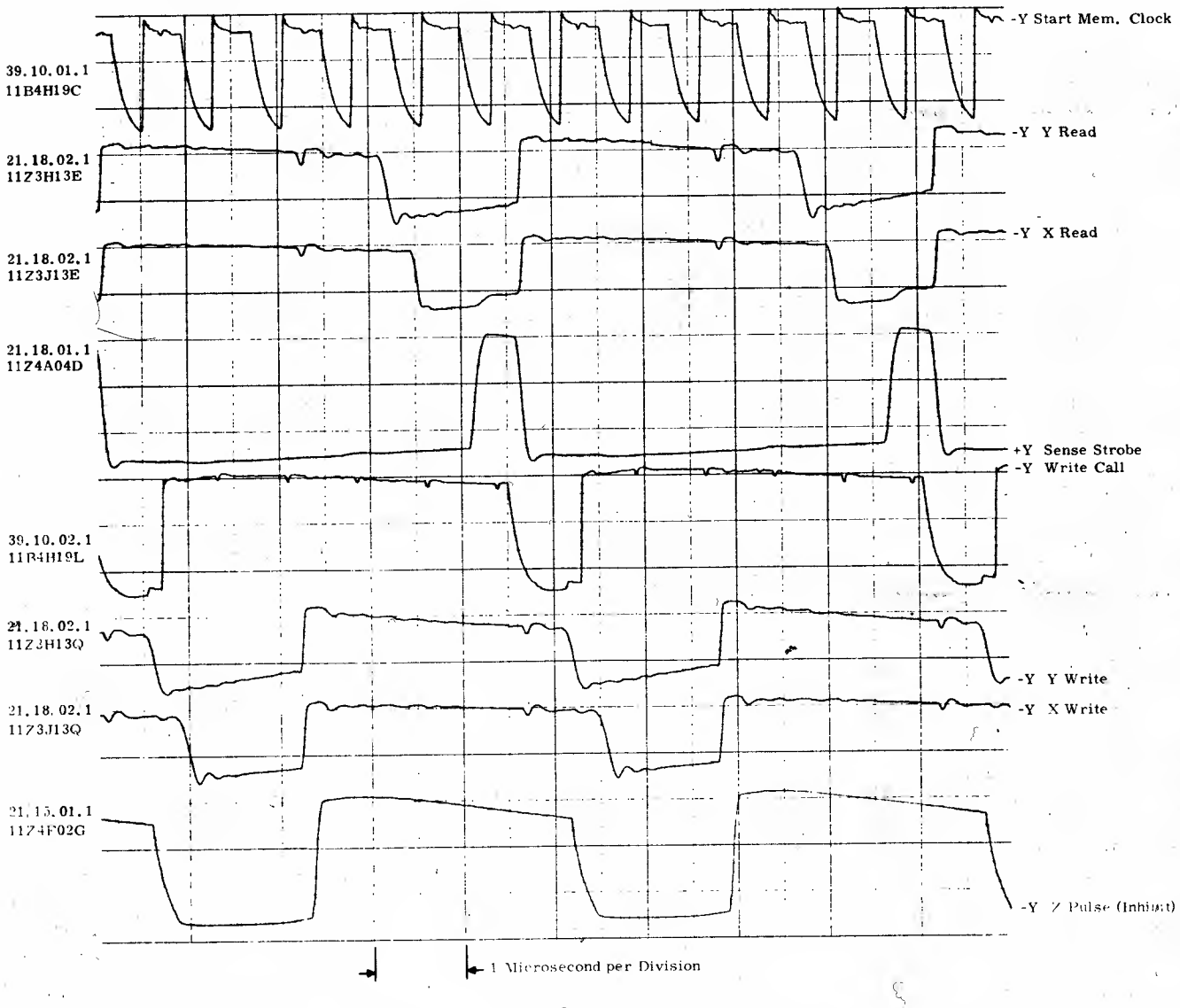


FIGURE 31-B Additional 60K Memory Timings

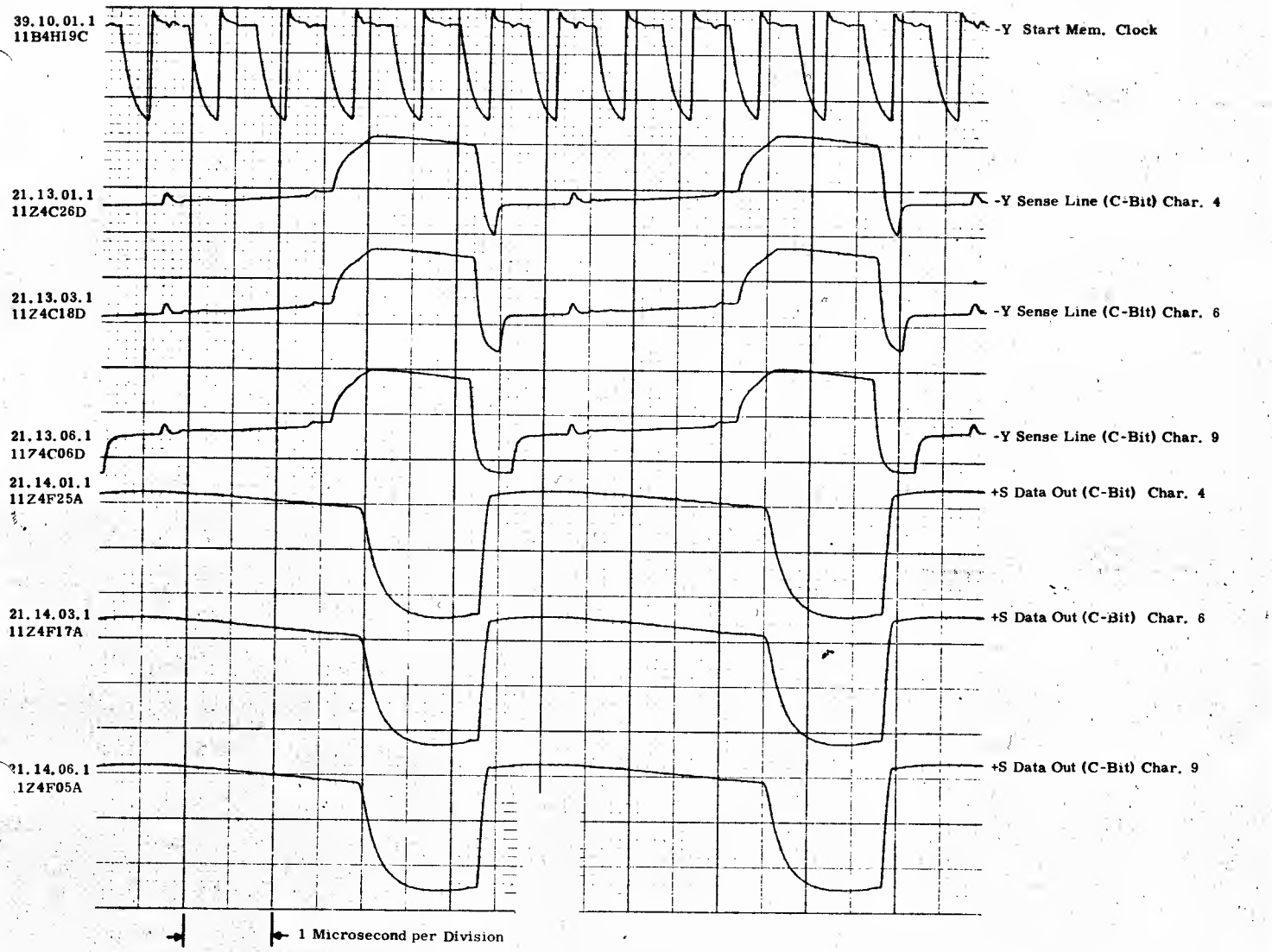


FIGURE 31-C Additional 60K Memory Timings

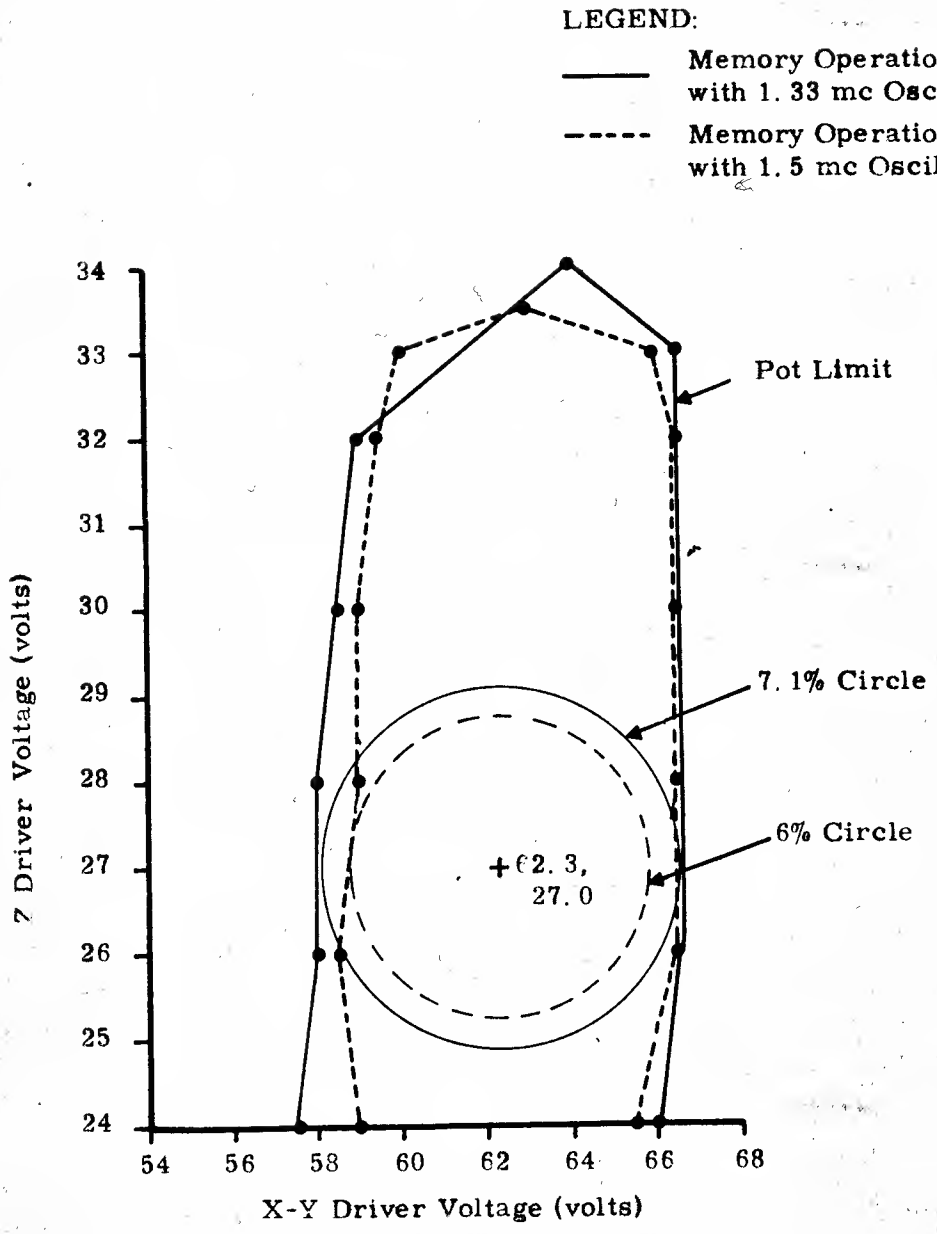


FIGURE 32 Additional 60K Memory Operational Limits with 1.33 MC and 1.5 MC Oscillator

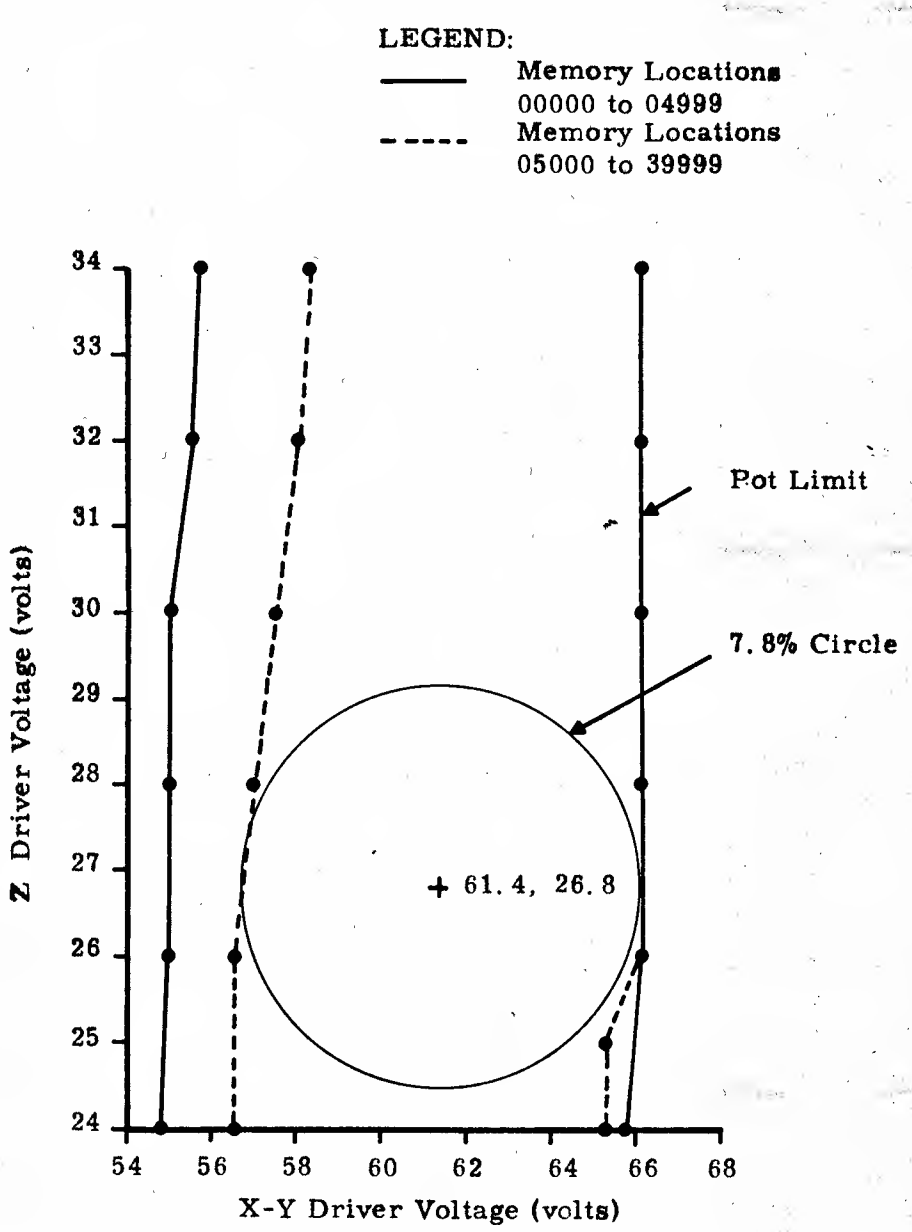


FIGURE 33 Basic 40K Memory Operational Limits with 1.33 MC Oscillator

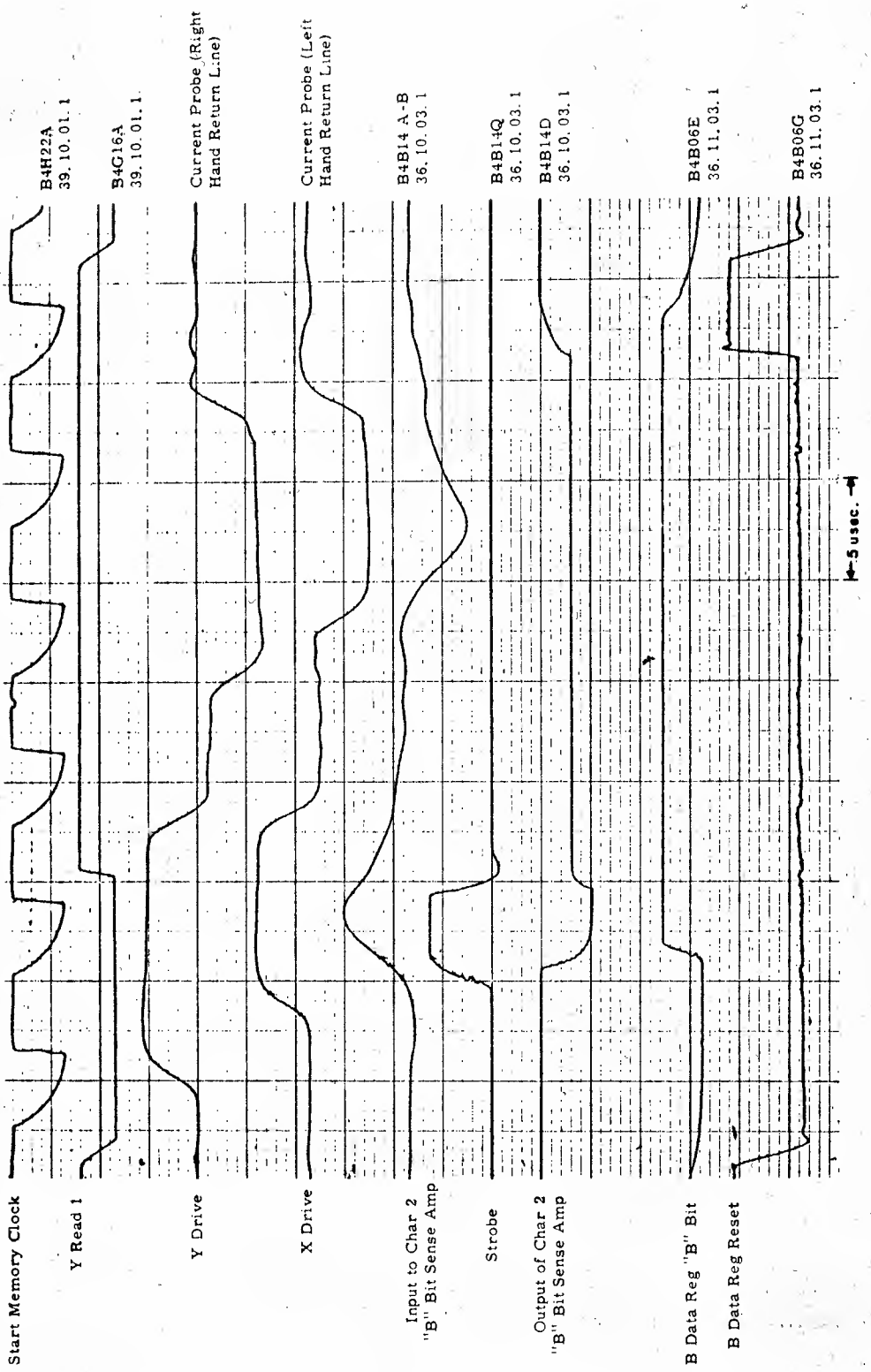


Figure 34 Standard 40K Memory, 1.33 Microsecond Oscillator Basic Read and Write Timings

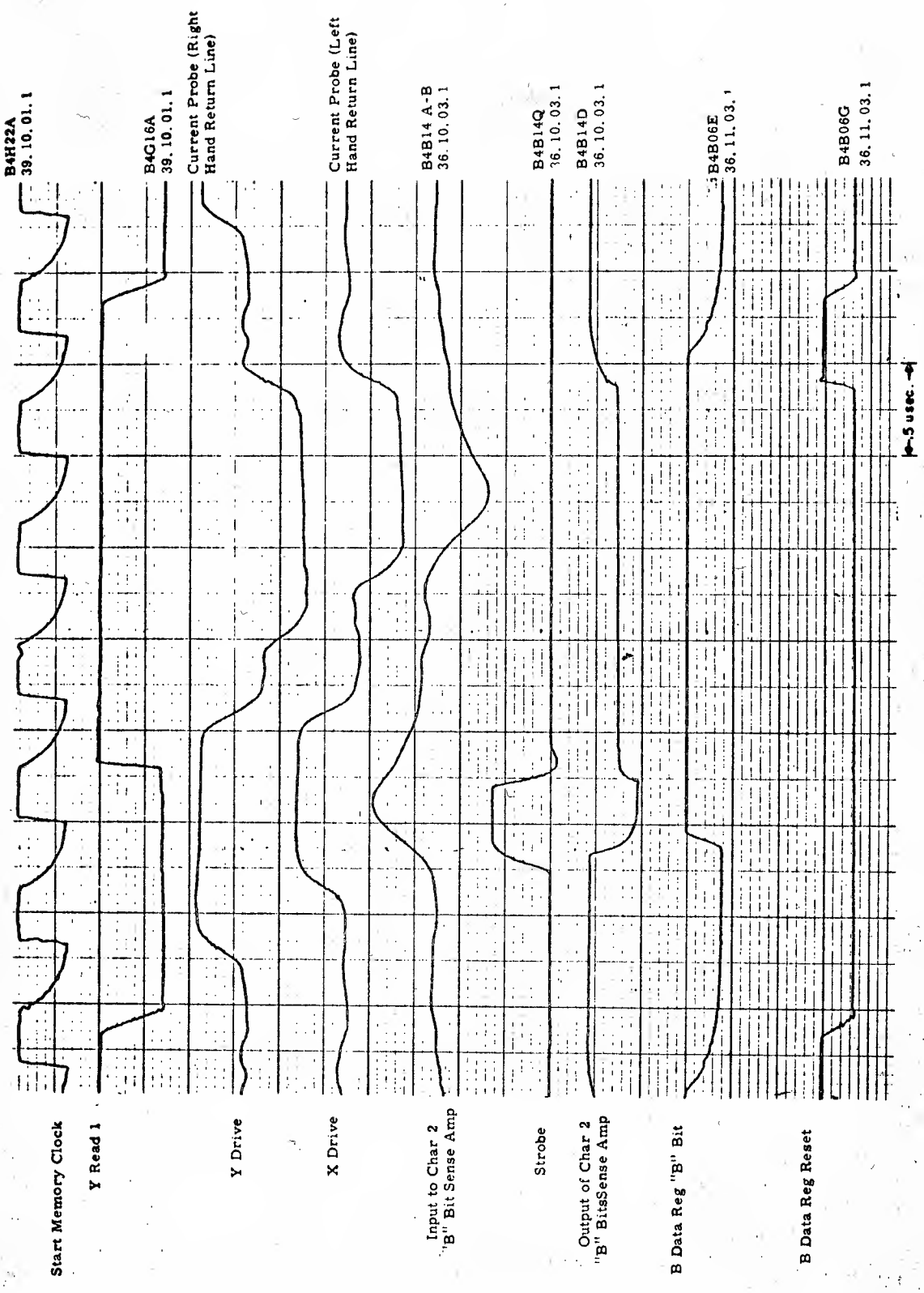


Figure 35 Standard 40K Memory, 1.5 Microsecond Oscillator Basic Read and Write Timings

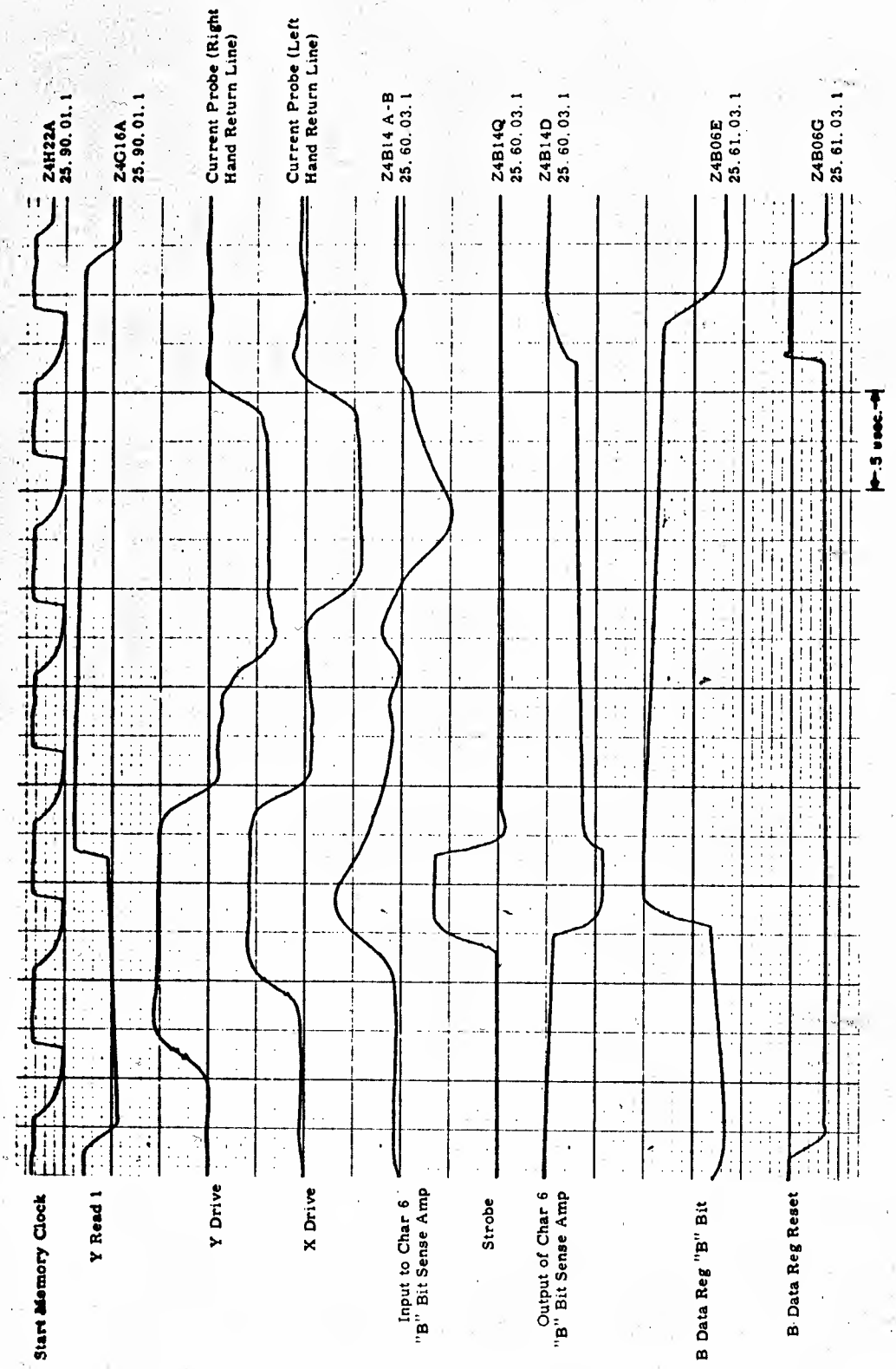


Figure 36 Additional 40K Memory 1.33 Microsecond Oscillator Basic Read and Write Timings

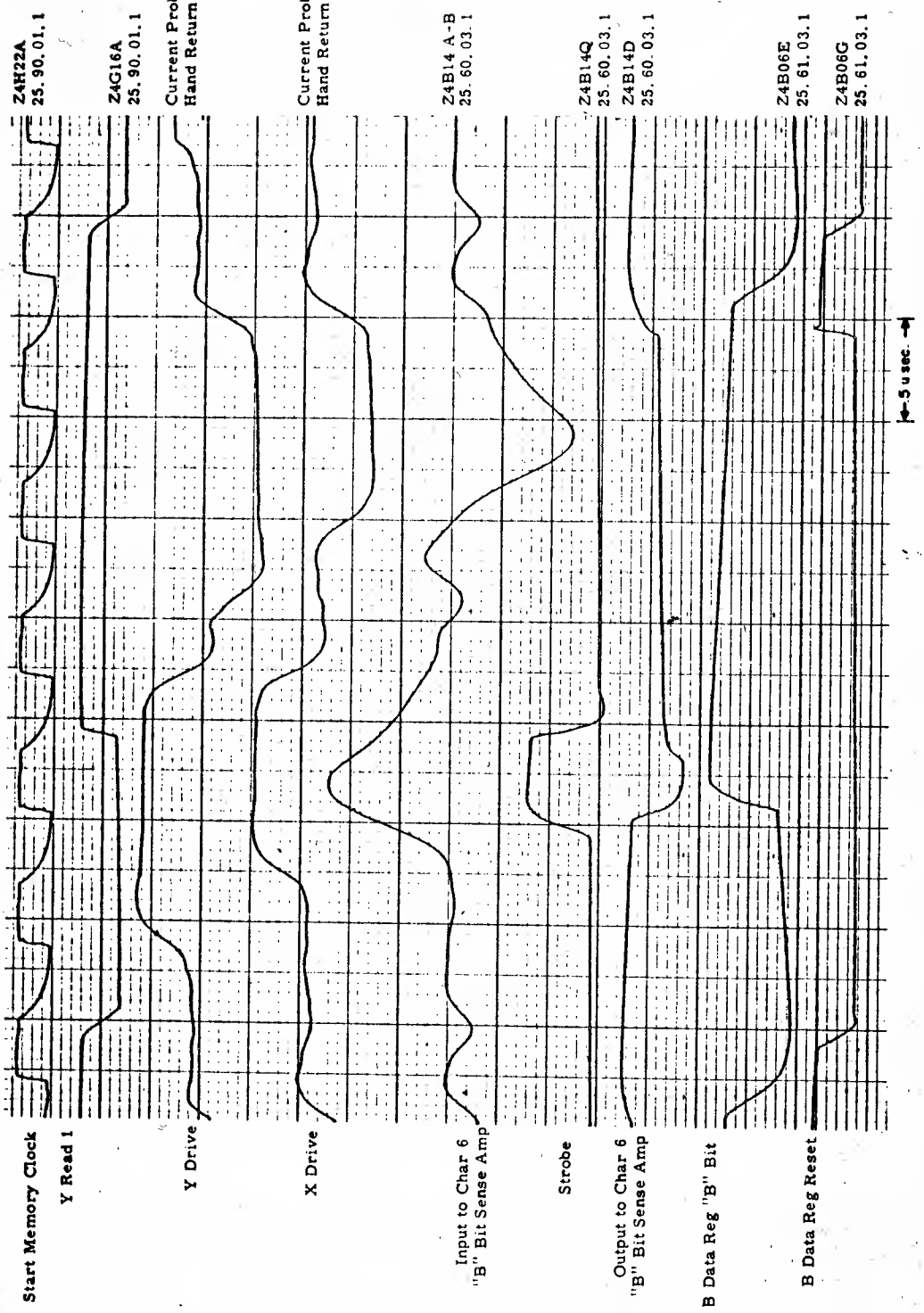


Figure 37 Additional 40K Memory, 1.5 Microsecond Oscillator Basic Read and Write Timings

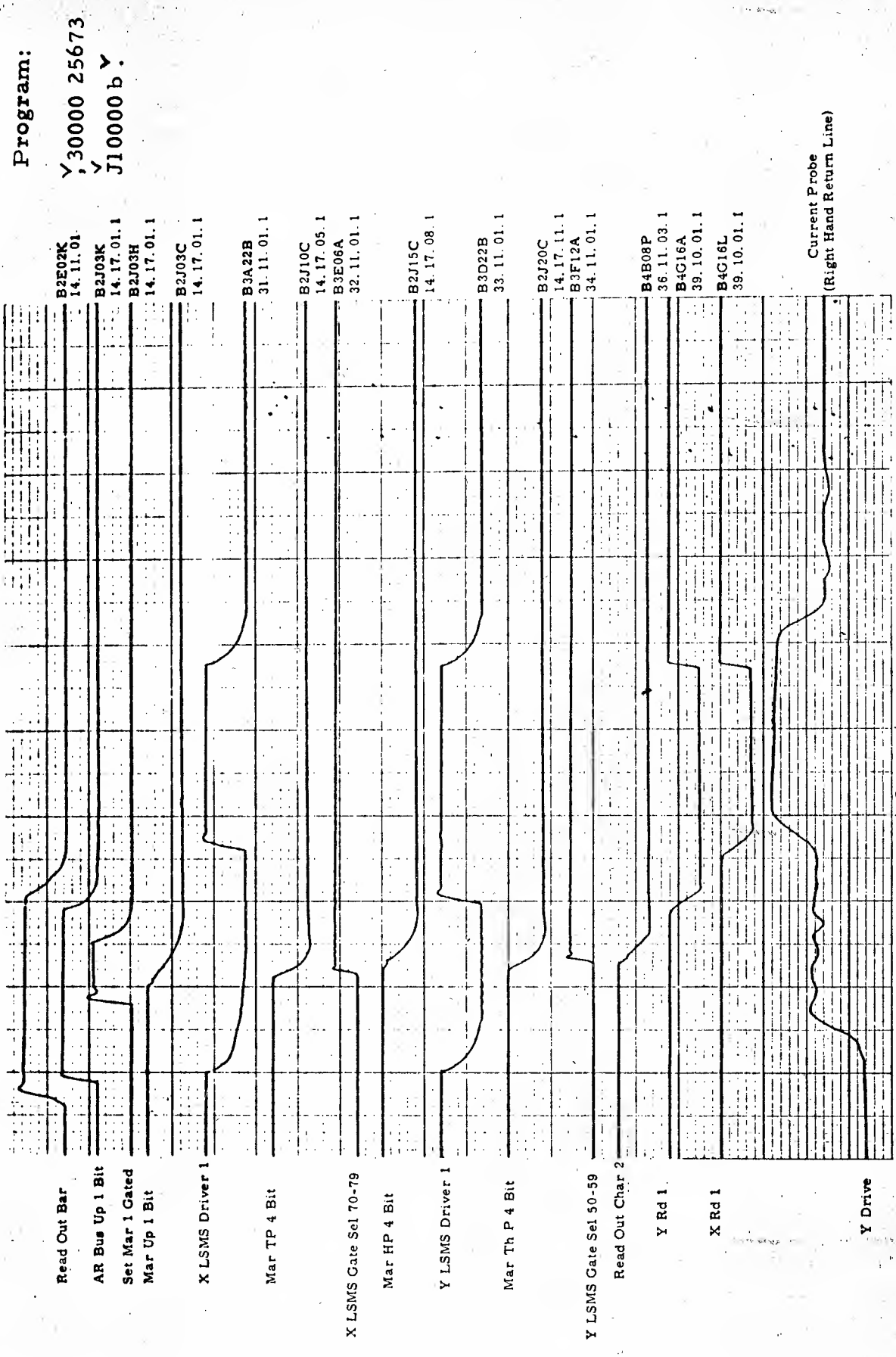


Figure 38 A Standard 40K Memory, 1.33 Microsecond Oscillator Character Read Out Timing

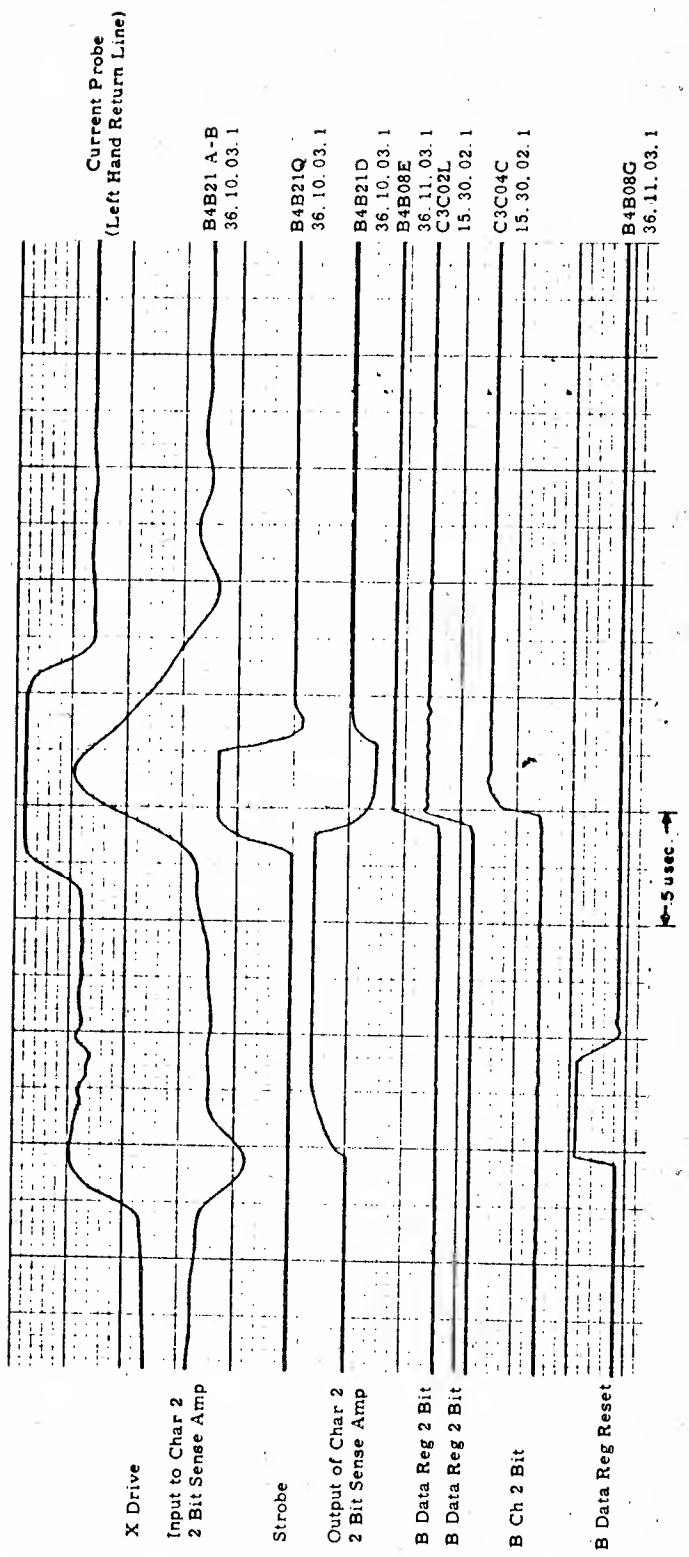


Figure 38 B Standard 40K Memory, 1.33 Microsecond Oscillator Character Read Out Timing - cont'd.

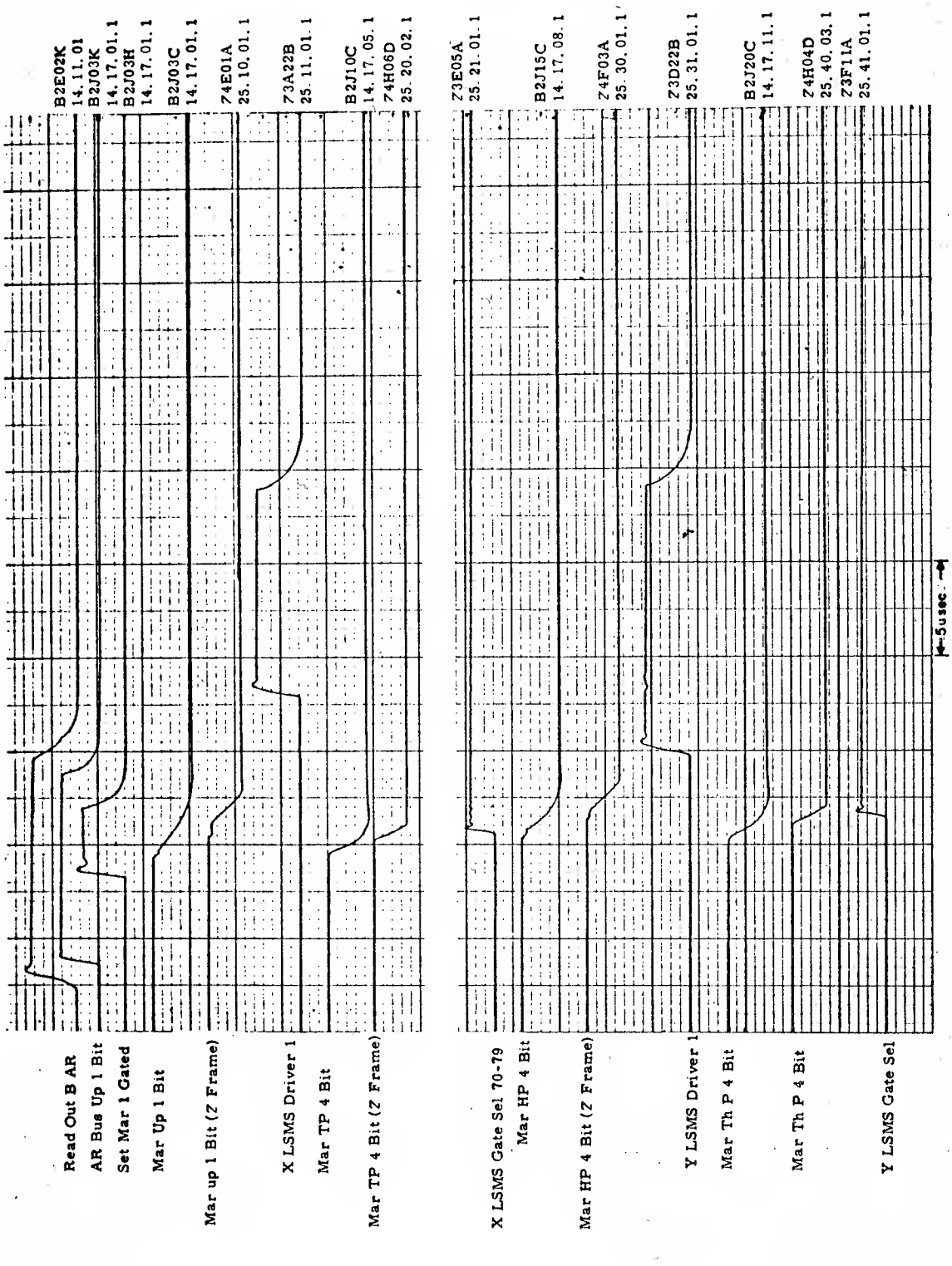


Figure 39 A Additional 40K Memory, 1.33 Microsecond Oscillator Character Read Out Timing

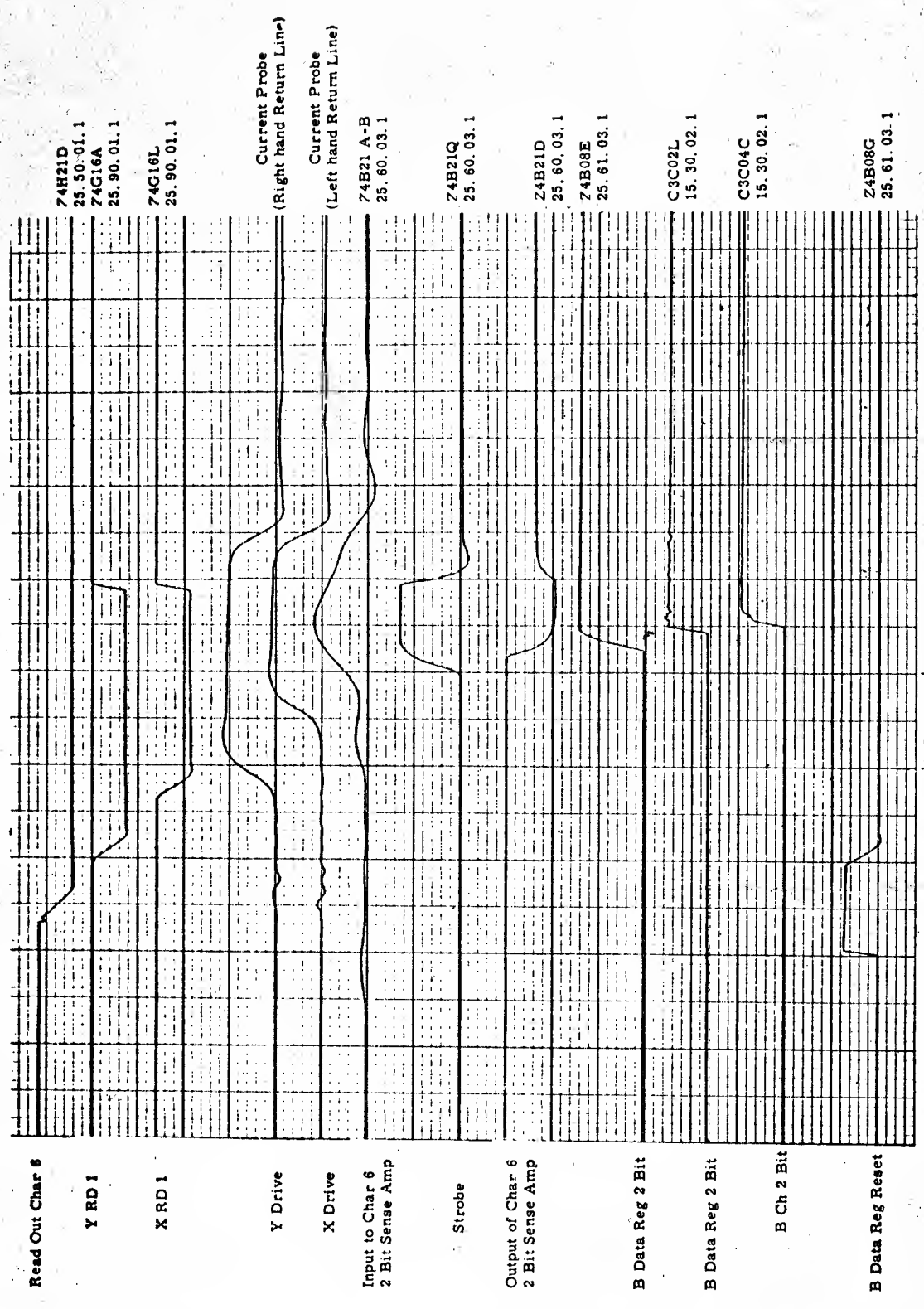


Figure 39 B Additional 40K Memory, 1.33 Microsecond Oscillator Character Read Out Timing - cont'd.

Address Failure Check

Solid errors due to faulty address switching may be quickly located by the following procedure. Use an address that will produce a fairly solid failure.

1. Place machine in Load +0, using a failing address.
2. Set scope for 20v/cm - 1us/cm.
3. Sync external on Read Call.
4. Adjust trace vertically for 0 volts at lowest graduation
5. Scope the 10X and 10Y LSMS power gates (only 5 Y gates on a 10K storage).

   Note: For each logical gate, there are two electrical gates, Pin Q and Pin R.

   Test points for X gates are: 11B3A01 Pins Q & R
   11B3A03 " "
   11B3A05 " "
   through 11B3A19 " "

   Test points for Y gates are: 11B3C01 Pins Q & R
   11B3C03 " "
   11B3C05 " "
   through 11B3C19 " "

6. There should be One logical X gate and One logical Y gate active. All other gates should be inactive.

   active level - approximately +12v to +15v

   inactive level - approximately +58v to +63v

7. If gates are correct, check the 16 X primary lines and the 16 Y primary lines, using the truth table (Systems 39.17.01 or Figure 14).

8. Check the 16 X lines at 11B3A01. Pins A through R are lines 16 through 1. Each line should pulse once during each storage cycle. If the truth table shows a Zero for primary line number four, this indicates that line number four should pulse during READ time. If the table shows a One for line number four, the line should pulse during WRITE time. All sixteen lines hould pulse once during each storage cycle, but eight should pulse during read time and the other eight should pulse during write time.

If gates and primaries are correct, check for shorted diodes, shorted windings or marginal timing conditions.

Driver Voltage Adjustments

The +60M and the +30M voltages must be adjusted to a value that is the best operating value for each particular core storage unit. This value is refered to as the nominal value, and will not necessarily be the same for any two core storage units. To find this nominal voltage setting, draw a graph, sometines referred to as a "schmoo" curve, as follows:

1. Power must be on for at least one hour before taking the test data.
2. Draw a scale for the 30VM and the 60VM supplies as shown in Figure 32, making the 30VM scale twice the scale used for the 60VM.
3. Adjust the +30 VM supply to 24V.
4. With diagnostic program C018C running, decrease the +60VM supply until the storage unit fails. Then increase the +60 VM supply in small increments (.25V) until the storage unit functions properly. Plot this +60VM value on the graph.

5. Increase the +60VM supply until the storage unit fails, then decrease the +60VM supply in small increments (.25V) until the unit functions properly and plot this value.
6. Increase the +30VM supply to 26 volts and repeat the procedure (steps 4 and 5) of finding the correct operating limits of the +60VM. Plot each limit of the +60VM at 2 volt +30VM increments until the +30VM reaches +34V.
7. Connect the points of the graph and draw the largest possible circle between the two lines.

The center of this circle is the nominal value for the +60VM and the +30VM. The size of this circle must be at least large enough to have a radius of 6% of the plotted value of the +60VM and th +30VM.

If this procedure is repeated periodically and the results recorded, any change in the size or center location of the circle is apparent and should be investigated.

Marginal Frequency Test

Once every six months check system operations at increased oscillator frequency for marginal characteristics, as follows:

1. Substitute a 1.5 mc oscillator card (part number 370823) for the standard oscillator card in chassis 1411 C 2, location H07.
2. Adjust the clock pulse delay-line so that the first and second clock pulses are 333 $\pm$ 40 nanoseconds wide. The interval from the 10% point of the rising edge of the second clock pulse to the 10% point of the rising edge of the first clock pulse is 333 $\pm$ 80 nanoseconds. The clock pulses should be measured at the output of the clock-pulse trigger inverters.

3. Run diagnostic program C 018C for 3 minutes at marginal voltages of 1.5 volts above and below nominal using J1, J3, and J4.

4. Replace the standard oscillator card and re-adjust the clock pulse delay-line so that:

   a. the second clock pulse is 375 $\pm$ 50 nsec.

   b. the first clock pulse is 375 $\pm$ 50 nsec.

   c. the interval between the 10% point of the rising edge of the 2nd clock pulse and the 10% point of the rising edge of the 1st clock pulse is 375 $\pm$ 100 nsec.

COMMENT SHEET

IBM 1410 CORE STORAGE – PRELIMINARY EDITION

CUSTOMER ENGINEERING INSTRUCTION-REFERENCE , FORM R23-2555

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